

標題	參考設計報告：使用 LinkSwitch™-HP LNK6774V 的 17 W 雙輸出返馳式轉換器，適用於 LCD 監視器
規格	90 VAC ~ 265 VAC 輸入； 5 V、1 A 和 18 V、670 mA 輸出
應用	LCD 監視器
作者	應用工程部門
文件編號	RDR-321
日期	2012 年 9 月 28 日
修訂	2.2

摘要與功能

- 一次側調節隔離式返馳式轉換器，調節範圍不超過 $\pm 5\%$
- 132 kHz 切換頻率，可減小變壓器和輸出濾波器的尺寸。
- 滿載連續導通模式操作，可改善效率並降低輸出電容器漣波電流
- 多重模式操作使滿載範圍內的效率達到最大
- 230 VAC 條件下，輸入功率低於 100 mW，待機功耗為 50 mW
- 廣泛的保護功能，包括 OVP、OTP、電壓啓動/關閉、線電壓過壓和喪失調節功能 (自動重新啓動)
- 符合 EN-550022 和 CISPR-22 B 級傳導性 EMI
- 符合 IEC61000-4-5 1 kV / 2 kV 突波標準

專利資訊

Power Integrations 的一項或多項美國及國外專利 (或可能正在申請的美國及國外專利) 可能涵蓋本文件中所示的產品和應用 (包括產品外部的變壓器構造和電路)。www.powerint.com 上提供了 Power Integrations 專利的完整清單。Power Integrations 授予其客戶某些特定專利權的授權，詳情請參閱 <<http://www.powerint.com/ip.htm>>。

Power Integrations

5245 Hellyer Avenue, San Jose, CA 95138 USA.

Tel:+1 408 414 9200 Fax: +1 408 414 9201

www.powerint.com

目錄

1	簡介	4
2	電源供應器規格	5
3	電路圖.....	7
4	電路說明	8
4.1	輸入整流和濾波	8
4.2	LinkSwitch-HP 一次側	8
4.3	一次側 RCD 箝位.....	8
4.4	輸出整流.....	8
4.5	外部限電流設定	9
4.6	回授和補償網路	9
5	PCB 佈局.....	10
6	物料表.....	11
7	變壓器設計試算表.....	12
8	變壓器規格.....	16
8.1	電氣圖.....	16
8.2	電氣規格	16
8.3	物料	16
8.4	變壓器建構圖：	17
8.5	變壓器構造：	17
8.6	變壓器示意圖：	18
9	效能資料	24
9.1	工作模式效率.....	24
9.2	待機輸入功率和待機效率.....	26
9.3	在 18 V 0.67 A DC 負載和 5 V 1 A 平均負載條件下的線電壓調節	28
9.4	指定動態負載輪廓 (包括峰值、最小值和平均值) 下的輸出電壓	30
9.4.1	峰值和最小輸出電壓的測試方法	30
9.4.2	指定負載輪廓下的 5 V 輸出電壓	31
9.4.3	指定負載配置下的 18 V 輸出電壓	35
10	散熱效能.....	39
11	波形.....	41
11.1	汲極電壓和電流，正常操作 on.....	41
11.2	汲極電壓和電流啓動配置	41
11.3	書出電壓啓動配置 (含輸入電壓).....	42
11.4	5 V 負載動態反應	43
11.4.1	使用 5 V 500 mA 至 1500 mA 步階負載和固定 18 V, 0.67 A DC 負載進行 5 V 動態測試.....	43
11.4.2	使用指定負載配置的 5 V 動態測試	44
11.4.3	使用指定負載配置的 18 V 動態測試	45
11.5	輸出漣波和雜訊測量.....	46



11.5.1	漣波測量技術.....	46
11.5.2	18 V 最大負載和 5 V 1 A 穩定負載下測試 18 V 的漣波.....	47
11.5.3	18 最大負載和 5 V 1 A 穩定負載下測試 5 V 的漣波.....	48
12	保護功能.....	49
12.1	短路自動重新啓動.....	49
12.2	輸出過壓保護.....	49
12.3	電壓啓動和電壓關閉測試.....	50
13	線電壓突波.....	51
14	ESD.....	51
15	滿載時的 EMI 測試.....	52
16	修訂記錄.....	54

重要附註：

雖然此電路板的設計滿足安全隔離需求，但其工程原型未經相關機構核准。因此，執行所有測試應使用隔離變壓器才能提供 AC 輸入給原型板。



1 簡介

本報告說明通用電壓輸入、5 V/1000 mA 和 18 V/670 mA 隔離式返馳式轉換器，採用 LinkSwitch-HP IC 系列中的 LNK6774V 裝置。內容涵蓋電源供應器的完整規格、詳細電路圖、打造供電器的完整物料清單、各種變壓器文件，以及最重要的電氣波形的測試資料和波形繪製圖。

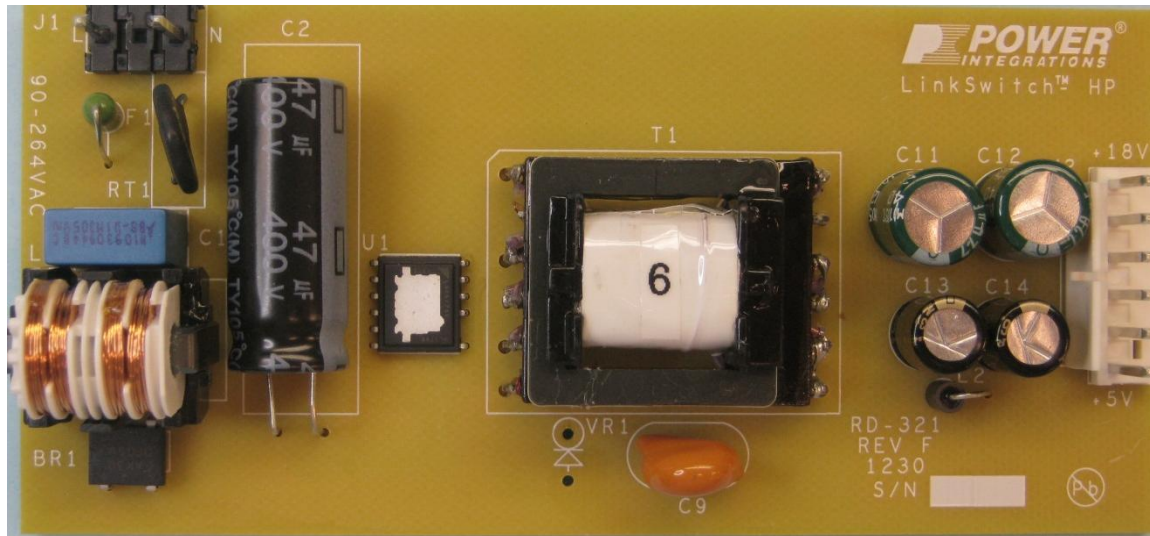


Figure 1 – Prototype Top View.

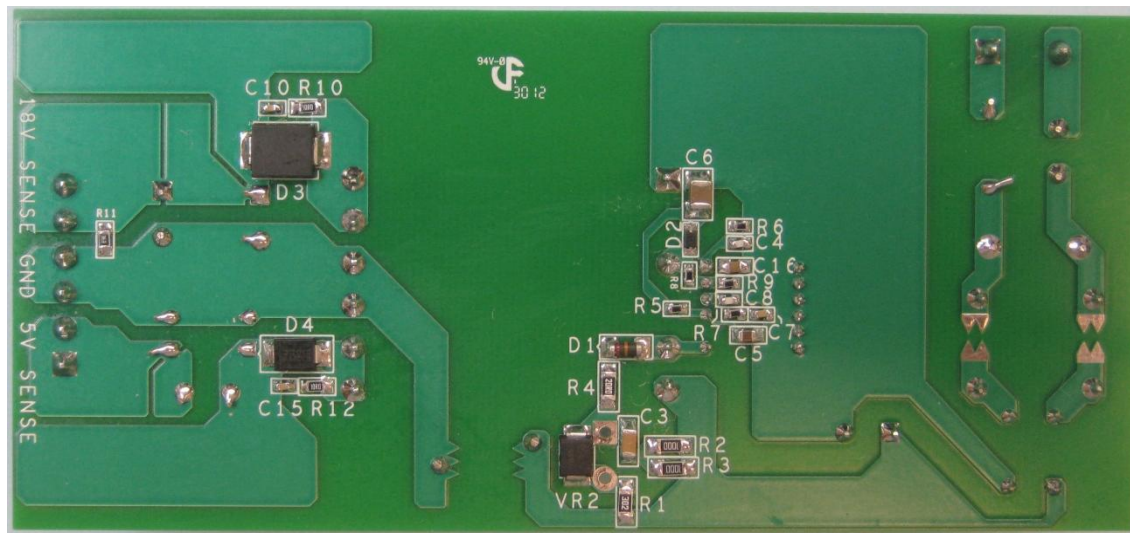


Figure 2 – Prototype Bottom View.

2 電源供應器規格

下表列出可接受此設計的最低效能。實際效能列在結果部分。

說明	符號	最小值	類型	最大值	單位	註解
輸入						
電壓	V_{IN}	90		265	VAC	雙線 – 無 P.E.
頻率	f_{LINE}	47	50/60	64	Hz	
待機輸入功率				100	mW	230 VAC、5 V 0.01 A、 18 V 無負載
輸出						
輸出電壓 1	V_{OUT1}	4.75	5	5.25	V	
輸出漣波電壓 1	$V_{RIPPLE1}$			100	mVpp	20 MHz 頻寬，含 穩態負載
輸出電流 1	I_{OUT1}	0.01		1500	mA	請參閱下面的負載輪廓圖
輸出電壓暫態 1	$V_{TRANSIENT1}$	4.75		5.5	V	請參閱下面的負載輪廓圖
輸出電壓 2	V_{OUT2}	16.2	18	26	V	
輸出漣波電壓 2	$V_{RIPPLE2}$				mV	20 MHz 頻寬
輸出電流 2	I_{OUT2}	0		670	mA	請參閱下面的負載輪廓圖
輸出電壓暫態 2	$V_{TRANSIENT2}$	16.2		28	V	請參閱下面的負載輪廓圖
總輸出功率						
連續輸出功率	P_{OUT}	0.05		17.1	W	
效率						
滿載效率	η	80			%	90 VAC 和滿載
環境						
傳導性 EMI		符合 CISPR22B / EN55015B 標準				
安全		設計符合 IEC950，UL1950 第 II 級標準				
突波	DM	1			kV	1.2/50 μ s 突波，IEC 1000-4-5， 串聯阻抗： 差模：2 Ω 共模：12 Ω
	CM	2				
ESD	空氣	-15		15	kV	在輸出連接器上空氣放電
	接觸	-6		6	kV	在輸出連接器上接觸放電
環境溫度	T_{AMB}	0		40	$^{\circ}$ C	自然對流，海平面



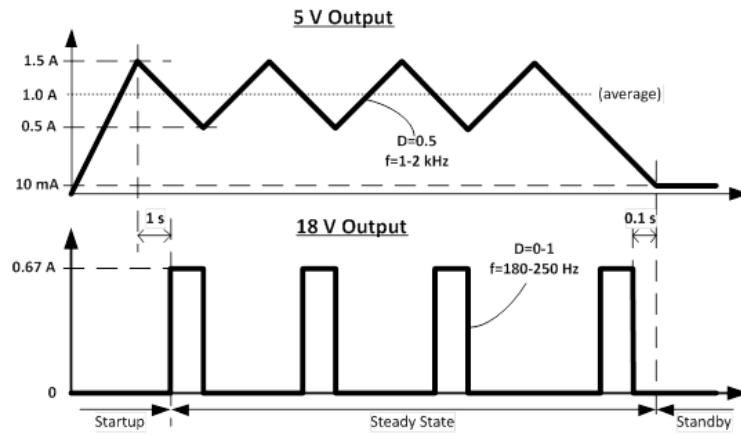


Figure 3 – Typical LCD Monitor Load Profile.



3 電路圖

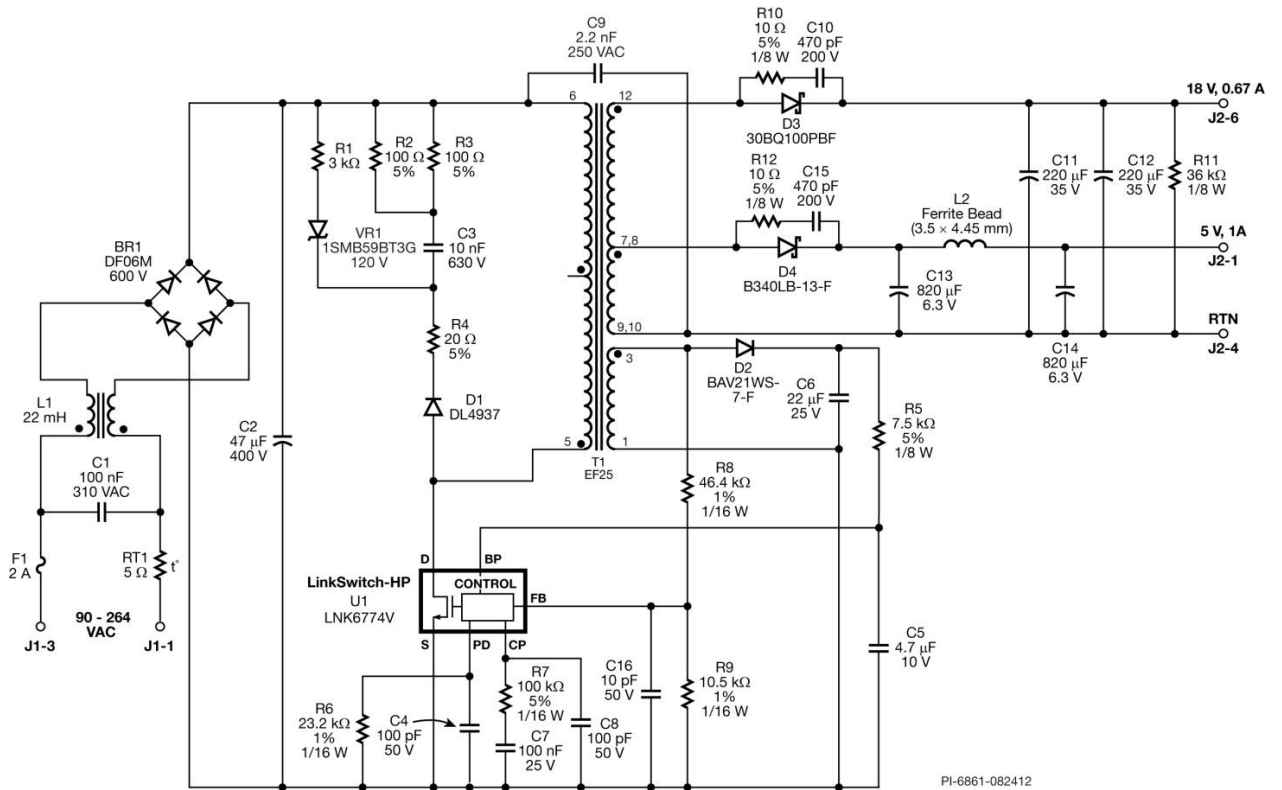


Figure 4 – Circuit Schematic.

4 電路說明

4.1 輸入整流和濾波

橋式整流器 BR1 會對 C2 過濾的 AC 輸入進行整流。電感器 L1、C1 和 C2 會用於削減差模和共模傳導性 EMI。遮蔽技術 (*E-Shield™*) 用於變壓器 T1 的構造中，以減少共模 EMI 位移電流。此濾波器排列、專利 E-Shield 技術加上 IC 的頻率抖動功能，為這個採用 Y 電容器和一次側 RCD 箝位電路的解決方案提供優異的 EMI 效能。

4.2 LinkSwitch-HP 一次側

LNK6774V 裝置 (U1) 將振盪器、誤差放大器和多模共用電路、啓動和保護電路，以及高壓功率 MOSFET 全都整合到一個單晶片 IC 上。

變壓器的一側連接到高壓匯流排，另一側則連接到 U1 的汲極接腳。在開始切換週期時，控制器會開啓功率 MOSFET，逐漸增加一次側繞組中的電流，藉此將能量儲存在變壓器的鐵芯。當電流達到內部誤差放大器 (CP 接腳電壓) 的輸出端所設定的限制臨界值，控制就會關閉功率 MOSFET。由於變壓器繞組的相位變化和輸出二極體的方向，儲存的能量會接著在二次側繞組上產生電壓，使輸出二極體變為正向偏壓，然後儲存的能量就會輸送到輸出電容器。

連接到 BP 接腳的電容器 C5 (4.7 μ F) 會設定過壓保護 (OVP)、喪失調節保護 (自動重新啓動)，以及過溫保護 (OTP)，以便在達到指定的關閉期間 (通常為 1500 ms) 之後自動嘗試重新啓動。其他組合包括鎖定 OTP 和 OVP 等，都可以設定搭配不同的電容器值。如需進一步的詳細資訊，請參閱 LinkSwitch-HP 規格型錄。

4.3 一次側 RCD 箝位

二極體 D1、VR1、C3、R1、R2、R3 和 R4 會形成 RCD 突波吸收器，以用於限制 LinkSwitch-HP 上的電壓應力。所以，265 VAC 條件下的汲極電壓峰值會限制為低於 580 V，這樣與汲極電壓 (BV_{DSS}) 725 V 之間就有很大的餘裕。積納二極體 VR1 會防止電容器 C3 完全放電每次切換週期，以降低待機功耗。

二極體 D1、R2、VR1、C3、R5 和 R6 會形成 RCD 突波吸收器，以用於限制 LinkSwitch-HP 上的電壓應力。所以，265 VAC 條件下的汲極電壓峰值會限制為低於 580 V，這樣與汲極電壓 (BV_{DSS}) 700 V 之間就有很大的餘裕。

4.4 輸出整流

對 18 V 輸出進行整流是由二極體 D3 所提供，濾波則由電容器 C11 和 C12 提供。R10 和 C10 形成的突波吸收器提供高頻率過濾，以改善 EMI。對 5 V 輸出進行整流是由二極體 D4 所提供，濾波則由電容器 C13 和 C14 及電感器 L2 提供。R12 和 C15 形成的突波吸收器提供高頻率過濾，以改善 EMI。



4.5 外部限電流設定

最大週期性電流限制是由連接至 PD 接腳的電阻器 R6 所設定。本設計中的 23.2 k Ω 電阻器將最大限電流設為 LNK6774V 預設限電流的 60%。

4.6 回授和補償網路

輸出電壓在返馳期間，會透過偏壓繞組和分壓電阻器 (R8 和 R9) 進行感測。感測到的輸出電壓會與 FB 接腳臨界值進行比較，以便調節輸出，或在偵測到過壓情況時停止切換 (OVP)。一次側調節解決方案不僅可降低系統成本，還可以改善系統使用期限，因為採用 LinkSwitch-HP 設計的電源供應器完全不需要光耦合器 (光耦合器會明顯降低電源供應器的使用期限)。

分壓電阻器 R8 和 R9 也會用於在整合功率 MOSFET 啟動期間，間接監控匯流排電壓。啟動時，此 IC 只會在匯流排達到 100 V (電壓關閉臨界值) 時才會啟用切換。假設例如在電壓關閉情況下，匯流排電壓下降至低於 40 V 典型值，則裝置會停止切換 (電壓關閉保護)。當匯流排電壓達到過大等級 (例如因為線電壓突波導致這情況)，則裝置會停止切換。此外，週期性電流限制會在線上補償，以限制可用的過載功率。如需進一步詳細資訊，請參閱裝置規格型錄。

在 FB 接腳處感測到的電壓會在 CP 接腳處產生控制電壓。電阻器 R7 和電容器 C7、C8 會用於控制迴路補償。一次側工作峰值電流和工作切換頻率由 CP 接腳電壓所決定。



5 PCB 佈局

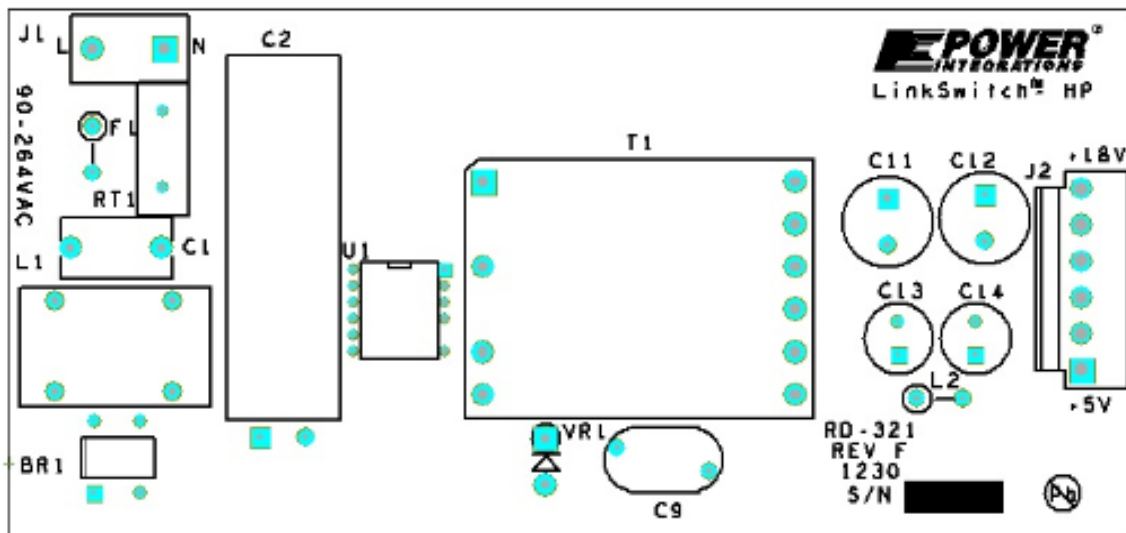


Figure 5 – PCB Top Side.

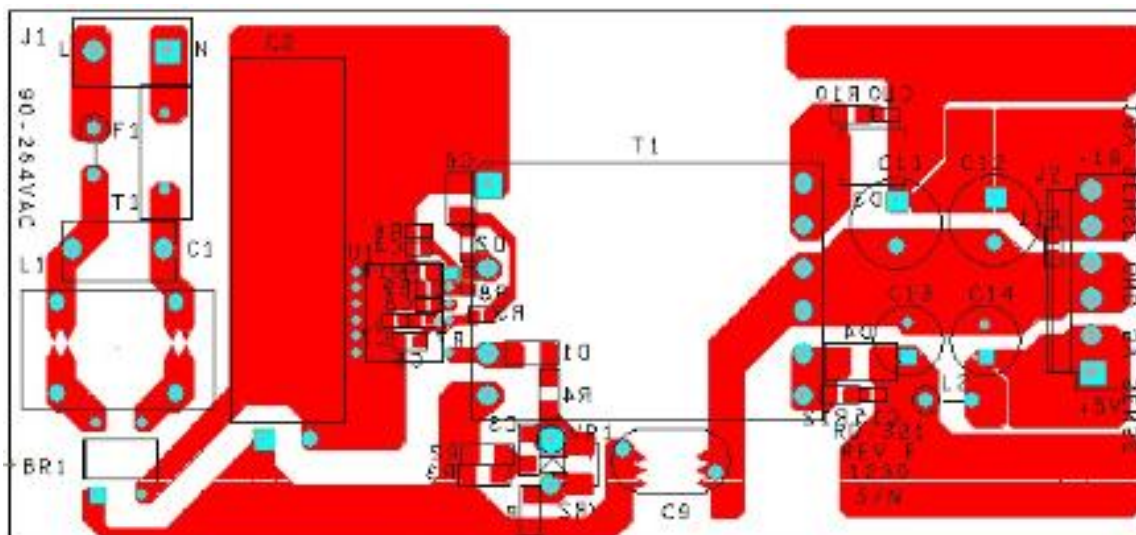


Figure 6 – PCB Bottom Side.

6 物料表

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	600 V, 1 A, Bridge Rectifier, DFM package	DF06M	Diodes, Inc.
2	1	C1	100 nF, 310 VAC, Film, X2	B32921C3104M	Epcos
3	1	C2	47 μ F, 400 V, Electrolytic, Low ESR, (12.5 x 30)	EPAG401ELL470MK30S	Nippon Chemi-Con
4	1	C3	10 nF, 630 V, Ceramic, X7R, 1206	C1206C103KBRACU	Kemet
5	2	C4 C8	100 pF 50 V, Ceramic, NPO, 0603	CC0603JRNPO9BN101	Yageo
6	1	C5	4.7 μ F, 10 V, Ceramic, X7R, 0805	C0805C475K8PACTU	Kemet
7	1	C6	22 μ F, 25 V, Ceramic, X5R, 1210	ECJ-4YB1E226M	Panasonic
8	1	C7	100 nF, 25 V, Ceramic, X7R, 0603	VJ0603Y104KNXAO	Vishay
9	1	C9	2.2 nF, Ceramic, Y1	440LD22-R	Vishay
10	2	C10 C15	470 pF, 200 V, Ceramic, X7R, 0603	06032C471KAT2A	AVX
11	2	C11 C12	220 μ F, 35 V, Electrolytic, Very Low ESR, 53 m Ω , (10 x 12.5)	EKZE350ELL221MJC5S	Nippon Chemi-Con
12	2	C13 C14	820 μ F, 6.3 V, Electrolytic, Low ESR, (8 x 11.5)	UHN0J821MPD	Nichicon
13	1	C16	10 pF, 50 V, Ceramic, NPO, 0805	ECJ-2VC1H100D	Panasonic
14	1	D1	600 V, 1 A, Rectifier, Fast Recovery, MELF (DL-41)	DL4937-13-F	Diodes, Inc.
15	1	D2	250 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV21WS-7-F	Diodes, Inc.
16	1	D3	100 V, 3 A, Schottky, SMC	30BQ100PBF	Vishay
17	1	D4	40 V, 3 A, Schottky, SMD, DO-214AA	B340LB-13-F	Diodes, Inc.
18	1	F1	Fuse, Pico, 2 A, 250 V, Fast, Axial	0263002.MXL	Littlefuse Inc.
19	1	J1	CONN HEADER 3POS (1x3).156 VERT TIN	26-64-4030	Molex
20	1	J2	CONN HEADER 6POS (1x6).156 VERT TIN	26-60-4060	Molex
21	1	L1	22 mH, 0.4 A, Common Mode Choke	ELF18D290C	Panasonic
22	1	L2	3.5 mm x 4.45 mm, 68 Ω at 100 MHz, #22 AWG hole, Ferrite Bead	2743001112	Fair-Rite
23	1	R1	3 k Ω , 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ302V	Panasonic
24	2	R2 R3	100 Ω , 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ 101V	Panasonic
25	1	R4	20 Ω , 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ 200V	Panasonic
26	1	R5	7.5 k Ω , 1%, 1/16 W, Thick Film, 0603	ERJ-3GEYJ 752V	Panasonic
27	1	R6	23.2 k Ω , 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF2322V	Panasonic
28	1	R7	100 k Ω , 5%, 1/16 W, Thick Film, 0603	ERJ-3GEYJ 104V	Panasonic
29	1	R8	46.4 k Ω , 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF4642V	Panasonic
30	1	R9	10.5 k Ω , 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1052V	Panasonic
31	2	R10 R12	10 Ω , 5%, 1/8 W, Thick Film, 0805	ERJ-6 GEYJ100V	Panasonic
32	1	R11	36 k Ω , 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ363V	Panasonic
33	1	RT1	NTC Thermistor, 5 Ohms, 4.7 A	CL-150	Thermometrics
34	1	T1	Bobbin, EF25, Horizontal, 12 pins Transformer	YC2504 SNX-R1652	Ying Chin Santronics USA
35	1	U1	LinkSwitch-HP, eDIP-12P	LNK6774V	Power Integrations
36	1	VR1	120 V, 550 mW, 5%, SMB, 403A	1SMB59xxBT3G	Semiconductor
37	1	VR2	OPEN	OPEN	



7 變壓器設計試算表

ACDC_LinkSwitch-HP_051612; Rev.0.13; Copyright Power Integrations 2012	INPUT	OUTPUT	UNIT	LinkSwitch-HP Flyback Transformer Design Spreadsheet
ENTER APPLICATION VARIABLES				
VACMIN	90	90	V	Minimum AC Input Voltage
VACMAX	265	265	V	Maximum AC Input Voltage
fL	50	50	Hz	AC Mains Frequency
VO	5	5	V	Output Voltage (main)
PO	17	17	W	Output Power
n	0.82	0.82		Efficiency Estimate
Z	0.50	0.50		Loss Allocation Factor
VB	10	10	V	Bias Voltage
tC	3	3	ms	Bridge Rectifier Conduction Time Estimate
CIN	47	47	uF	Input Filter Capacitor
ENTER LINKSWITCH-HP VARIABLES				
LinkSwitch-HP	LNK6774V		LNK6774V	
ILIMITMIN		0.967	A	Minimum Current limit
ILIMITMAX		1.113	A	Maximum current limit
KI	0.60	0.600	A	Current limit reduction factor
ILIMITMIN_EXT			0.580	A
ILIMITMAX_EXT			0.668	A
fS		132000	Hz	LinkSwitch-HP Switching Frequency:Choose between 132 kHz and 66 kHz
fSmin		124000	Hz	LinkSwitch-HP Minimum Switching Frequency
fSmax		140000	Hz	LinkSwitch-HP Maximum Switching Frequency
KP	0.5	0.50		Ripple to Peak Current Ratio (0.4 < KP < 6.0)
VOR	110	110.00	V	Reflected Output Voltage
Voltage Sense				
VUVON			100	100.00
VUVOFF			42.55	V
VOV			446.26	V
FMAX_FULL_LOAD		132885	Hz	Maximum switching frequency at full load
FMIN_FULL_LOAD		117698	Hz	Minimum switching frequency at full load
TSAMPLE_FULL_LOAD				
TSAMPLE_LIGHT_LOAD		1.77	us	Minimum available Diode conduction time at light load.This should be greater than 1.11 us



Rpd		23.20	k-ohm	Program delay Resistor
Cpd	10	10.00	nF	Program delay Capacitor
Total programmed delay		0.06	sec	Total program delay
VDS		4.11	V	LinkSwitch-HP on-state Drain to Source Voltage
VD				
VDB			0.70	V
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES				
Core Type	EF25			
Core		EF25		Selected Core
Custom Core				Enter name of custom core is applicable
AE	0.5180	0.518	cm^2	Core Effective Cross Sectional Area
LE	5.7800	5.78	cm	Core Effective Path Length
AL	2000.0	2000	nH/T^2	Ungapped Core Effective Inductance
BW	15.6	15.6	mm	Bobbin Physical Winding Width
M	0.00	0.00	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L			4.00	4
NS	3.00	3		Number of Secondary Turns
DC INPUT VOLTAGE PARAMETERS				
VMIN	85	85	V	Minmum DC Input Voltage
VMAX	375	375	V	Maximum DC Input Voltage
CURRENT WAVEFORM SHAPE PARAMETERS				
DMAX		0.58		Maximum Duty Cycle
Iavg		0.24	A	
IP		0.56	A	Peak Primary Current
IR				
IRMS		0.33	A	Primary RMS Current
TRANSFORMER PRIMARY DESIGN PARAMETERS				
LP_TYP		1436	uH	Typical Primary Inductance
LP_TOL	7	7	%	Primary inductance Tolerance
NP		60		Primary Winding Number of Turns
NB		6		Bias Winding Number of Turns
ALG		399	nH/T^2	Gapped Core Effective Inductance
BM		2607	Gauss	Maximum Flux Density at PO, VMIN (BM<3000)
BP		3301	Gauss	Peak Flux Density (BP<3700)
BAC		652	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)



ur		1776		Relative Permeability of Ungapped Core
LG		0.13	mm	Gap Length (Lg > 0.1 mm)
BWE		62.4	mm	Effective Bobbin Width
OD	0.32	0.32	mm	Maximum Primary Wire Diameter including insulation
INS		0.05	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA		0.27	mm	Bare conductor diameter
AWG		30	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM				
CMA		310	Cmils/Amp	Primary Winding Current Capacity (200 < CMA < 500)
FEEDBACK SENSING SECTION				
RFB1		37.40	k-ohms	Feedback divider upper resistor
RFB2				
TRANSFORMER SECONDARY DESIGN PARAMETERS (SINGLE OUTPUT EQUIVALENT)				
Lumped parameters				
ISP		11.29	A	Peak Secondary Current
ISRMS		5.61	A	Secondary RMS Current
IO		3.40	A	Power Supply Output Current
IRIPPLE		4.46	A	Output Capacitor RMS Ripple Current
CMS		1122	Cmils	Secondary Bare Conductor minimum circular mils
AWGS		19	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
DIAS		0.91	mm	Secondary Minimum Bare Conductor Diameter
ODS				5.20
INSS		2.14	mm	Maximum Secondary Insulation Wall Thickness
VOLTAGE STRESS PARAMETERS				
VDRAIN		626	V	Peak voltage across drain to source of Linkswitch-HP
PIVS		24	V	Output Rectifier Maximum Peak Inverse Voltage
PIVB				
TRANSFORMER SECONDARY DESIGN PARAMETERS (MULTIPLE OUTPUTS)				
1st output				
VO1	5.00	5	V	Output Voltage
IO1	1.00	1.00	A	Output DC Current
PO1		5.00	W	Output Power
VD1	0.35	0.35	V	Output Diode Forward Voltage Drop
NS1		2.92		Output Winding Number of Turns
ISRMS1		1.651	A	Output Winding RMS Current



IRIPPLE1		1.31	A	Output Capacitor RMS Ripple Current
PIVS1		23	V	Output Rectifier Maximum Peak Inverse Voltage
CMS1		330	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS1		24	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS1		0.51	mm	Minimum Bare Conductor Diameter
ODS1		5.35	mm	Maximum Outside Diameter for Triple Insulated Wire
2nd output				
VO2	18.00		V	Output Voltage
IO2	0.67		A	Output DC Current
PO2		12.06	W	Output Power
VD2	0.50	0.5	V	Output Diode Forward Voltage Drop
NS2		10.09		Output Winding Number of Turns
SRMS2		1.106	A	Output Winding RMS Current
IRIPPLE2		0.88	A	Output Capacitor RMS Ripple Current
PIVS2		81	V	Output Rectifier Maximum Peak Inverse Voltage
CMS2		221	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS2		26	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS2		0.41	mm	Minimum Bare Conductor Diameter
ODS2		1.55	mm	Maximum Outside Diameter for Triple Insulated Wire



8 變壓器規格

8.1 電氣圖

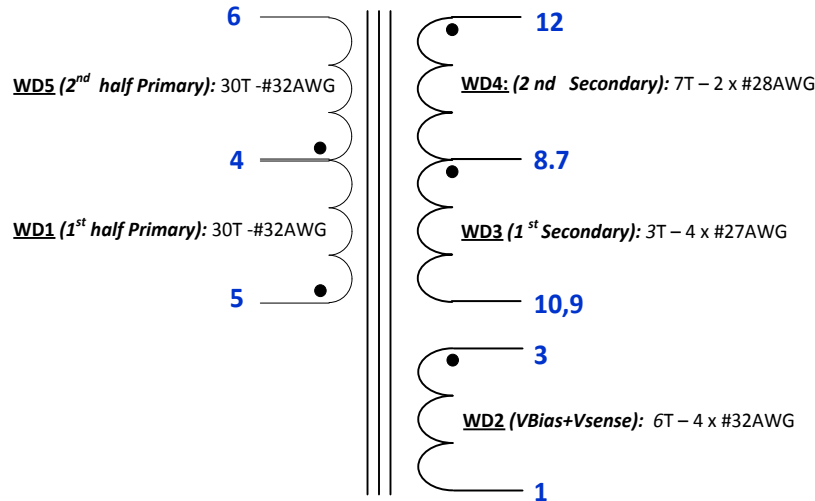


Figure 7 – Transformer Electrical Diagram.

8.2 電氣規格

Electrical Strength	1 second, 60 Hz, from pins 1-6 and pins 7-12.	3000 VAC
Primary Inductance	Pins 5-6, all other windings open, measured at 100 kHz, 0.4 VRMS.	1436 μ H \pm 7%
Resonant Frequency	Pins 5-6, all other windings open.	1500 kHz (Min.)
Primary Leakage Inductance	Pins 5-6, with pins 7-12 shorted, measured at 100 kHz, 0.4 VRMS.	15 μ H (Max.)

8.3 物料

Item	Description
[1]	Core:EF25, TDK PC44-EF25Z, and gapped ALG 398.9 nH/T ² .
[2]	Bobbin:EF25-Horizontal, 12 pins (6/6), Ying Chin, P/N:YC-2504.
[3]	Magnet wire:#32 AWG Solderable, double coated.
[4]	Magnet wire:#27 AWG Solderable, double coated.
[5]	Magnet wire:#28 AWG Solderable, double coated.
[6]	Teflon tube:Alpha Wire, TFT, or equivalent.
[7]	Tape:3M 44 Margin tape (cream), 3.5 mm wide, or equivalent.
[8]	Tape:3M 1298 Polyester Film, 8.6 mm wide, 2.0 mils thick, or equivalent.
[9]	Tape:3M 1298 Polyester Film, 15.6 mm wide, 2.0 mils thick, or equivalent.
[10]	Varnish:Dolph BC-359, or equivalent.



8.4 變壓器建構圖：

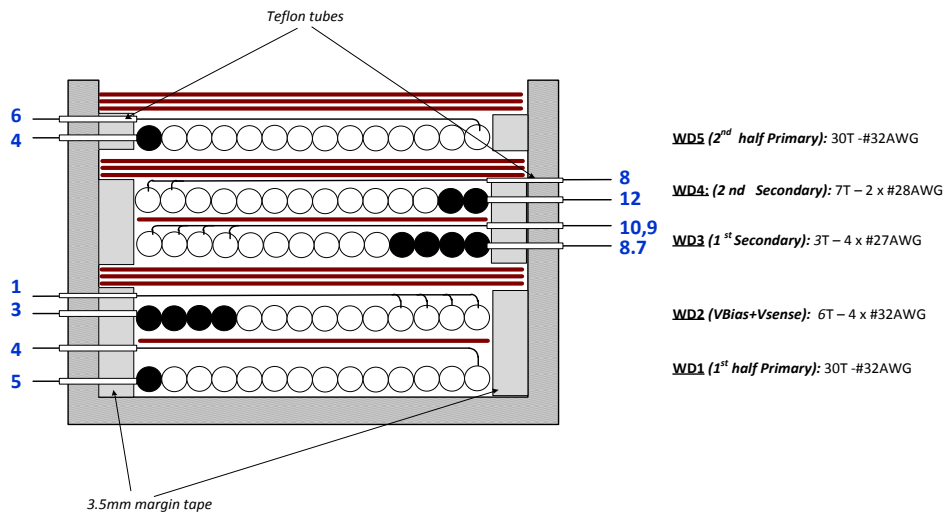


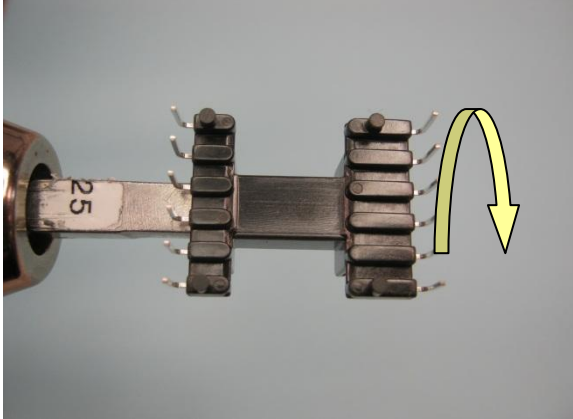
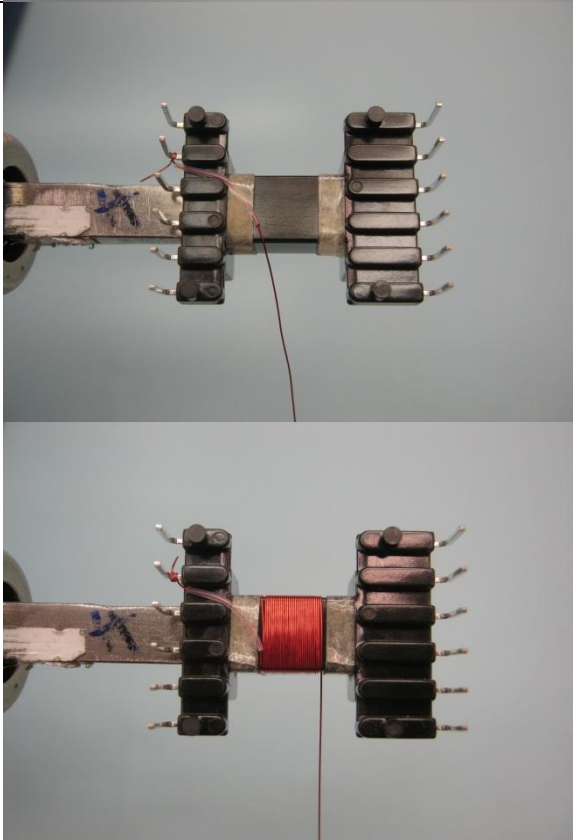
Figure 8 – Transformer Build Diagram.

8.5 變壓器構造：

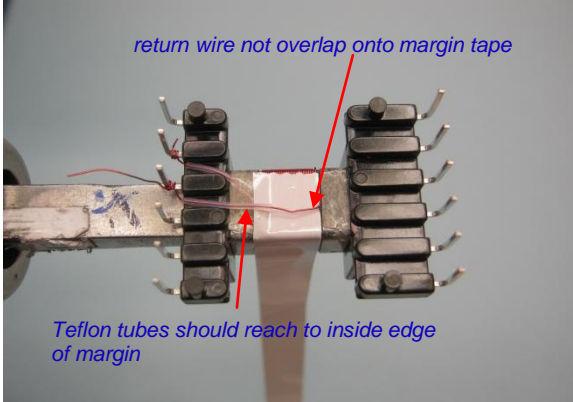
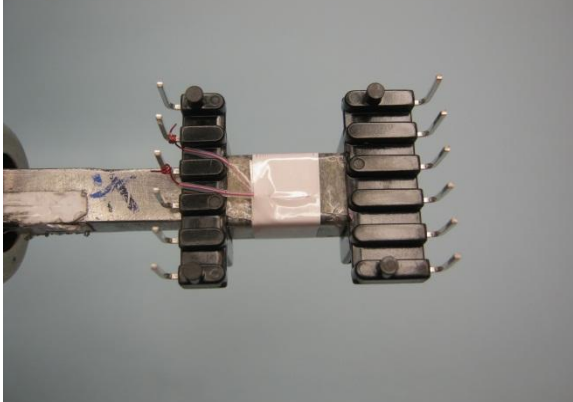
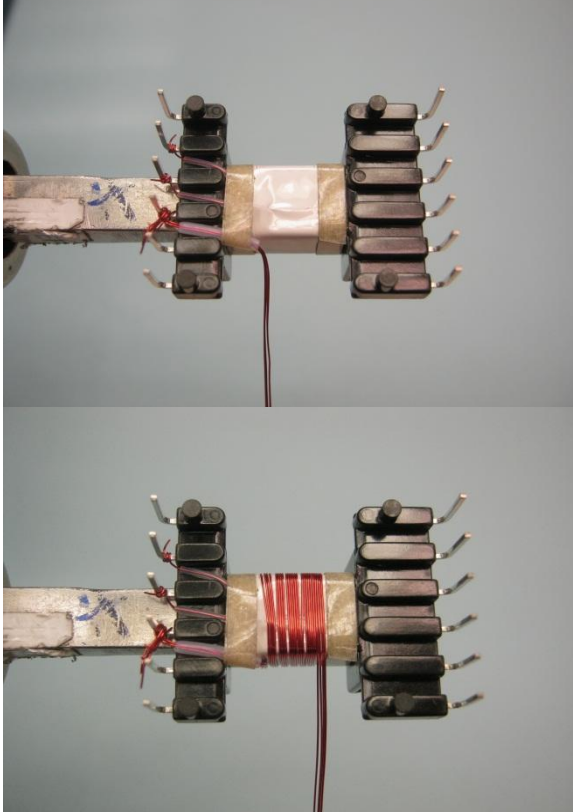
Winding preparation	Place the bobbin item [2] on the mandrel with the primary side is on the left side. Winding direction is clockwise direction. Margin tape item [7] should be applied for all windings. <u>Note:</u> Teflon tubes item [6] should be inserted into all wire ends and reach to inside edge of margin tapes. Return wires should be inside the winding section and not overlap on the margin tape. (See pictures below).
WD1 1st Half Primary	Start at pin 5, wind 30 turns of wire item [3] from left to right with tight tension, at the last turn bring the wire back to the left, and terminate at pin 4.
Insulation	Place 1 layer of tape item [8].
WD2 VBias+VSense	Start at pin 3, wind 6 quad-filar turns of wire item [3] from left to right with tight tension, at the last turn bring the wire back to the left, and terminate at pin 1.
Insulation	Place 3 layers of tape item [9].
WD3 1st Secondary	Start at pins 8,7, wind 3 quad-filar turns of wire item [4] from right to left, spread the wire evenly, at the last turn bring the wire back to the right, and terminate at pin 10,9.
Insulation	Place 1 layer of tape item [8].
WD4 2nd Secondary	Start at pins 12, wind 7 bi-filar turns of wire item [5] from right to left, spread the wire evenly, at the last turn bring the wire back to the right, and terminate at pin 8.
Insulation	Place 3 layers of tape item [9].
WD5 2nd Half Primary	Start at pin 4, wind 30 turns of wire item [3] from left to right with tight tension, at the last turn bring the wire back to the left, and terminate at pin 6.
Final Assembly	Grind and secure core halves with tape. Vanish item [10].

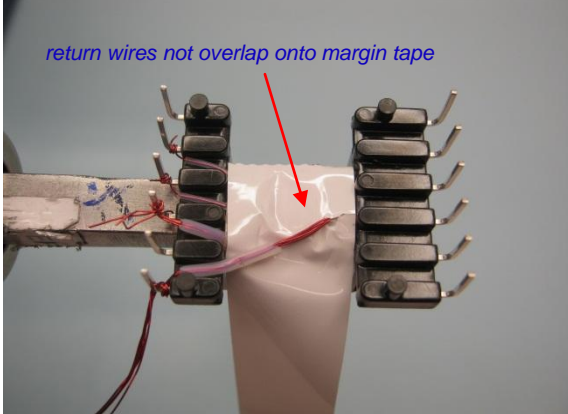
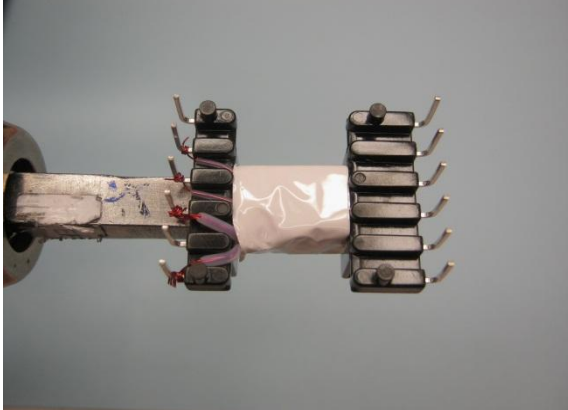
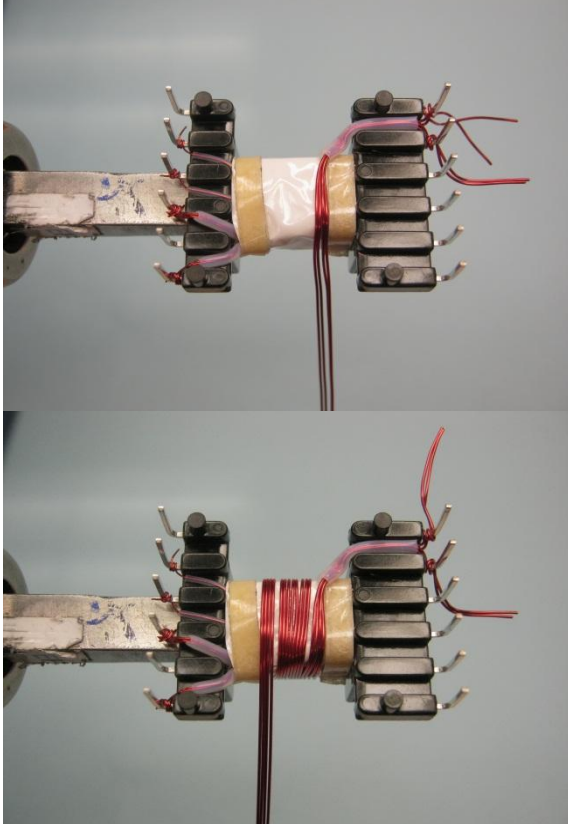


8.6 變壓器示意圖：

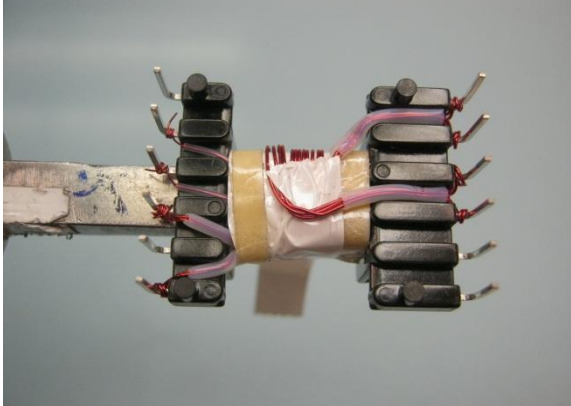
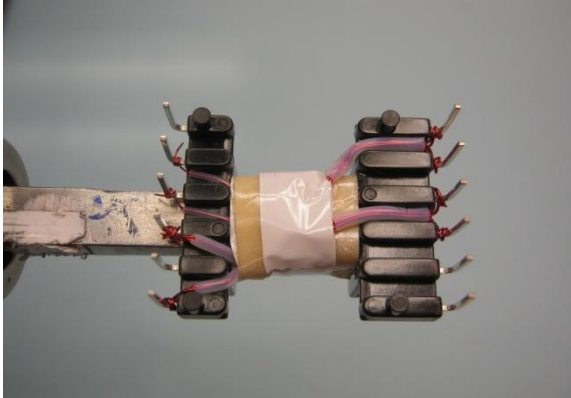
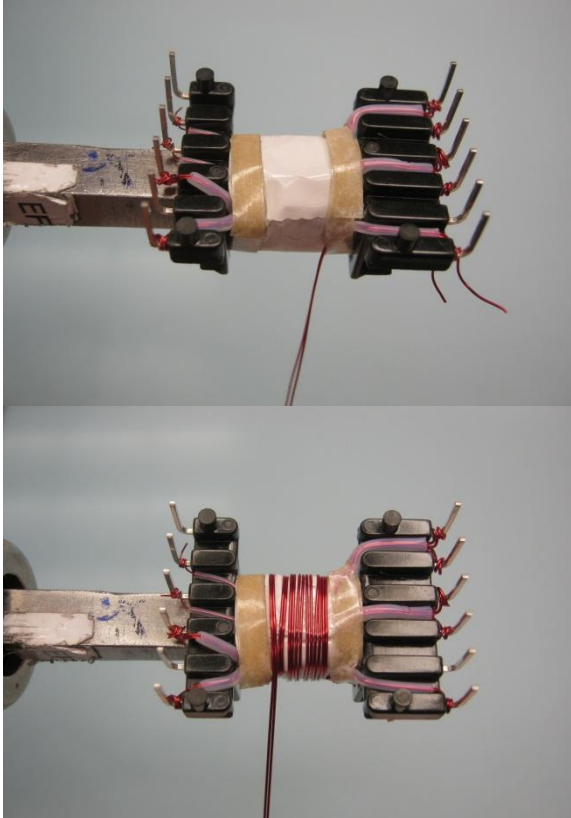
<p>Winding Preparation</p>		<p>Place the bobbin item [2] on the mandrel with the primary-side is on the left side. Winding direction is clockwise direction.</p>
<p>WD1 1st Half Primary</p>		<p>Start at pin 5, wind 30 turns of wire item [3] from left to right with tight tension, at the last turn bring the wire back to the left, and terminate at pin 4.</p>

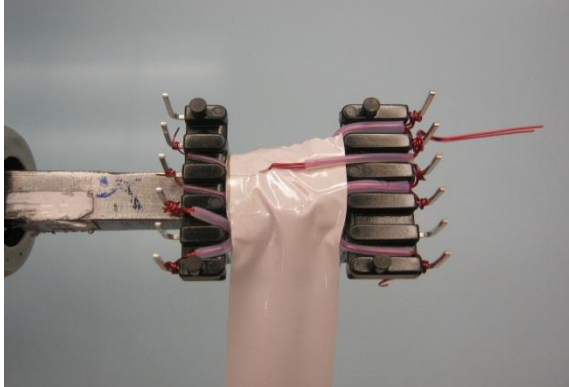
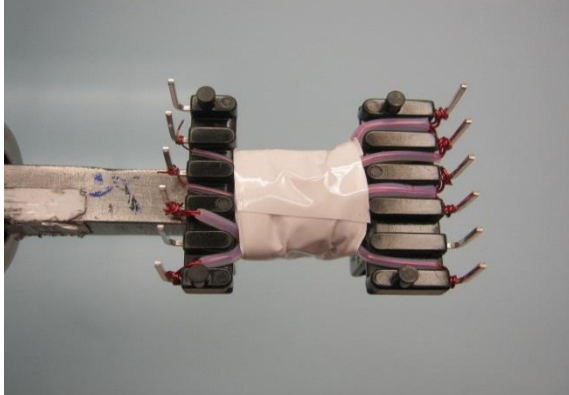
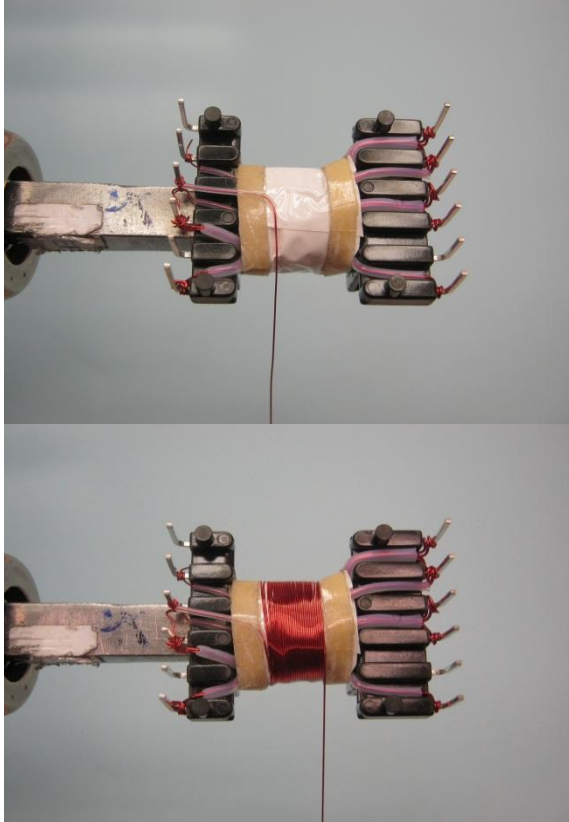


	 <p><i>return wire not overlap onto margin tape</i></p> <p><i>Teflon tubes should reach to inside edge of margin</i></p>	
<p>Insulation</p>		<p>Place 1 layer of tape item [8].</p>
<p>WD2 VBias+VSense</p>		<p>Start at pin 3, wind 6 quad-filar turns of wire item [3] from left to right with tight tension,</p>

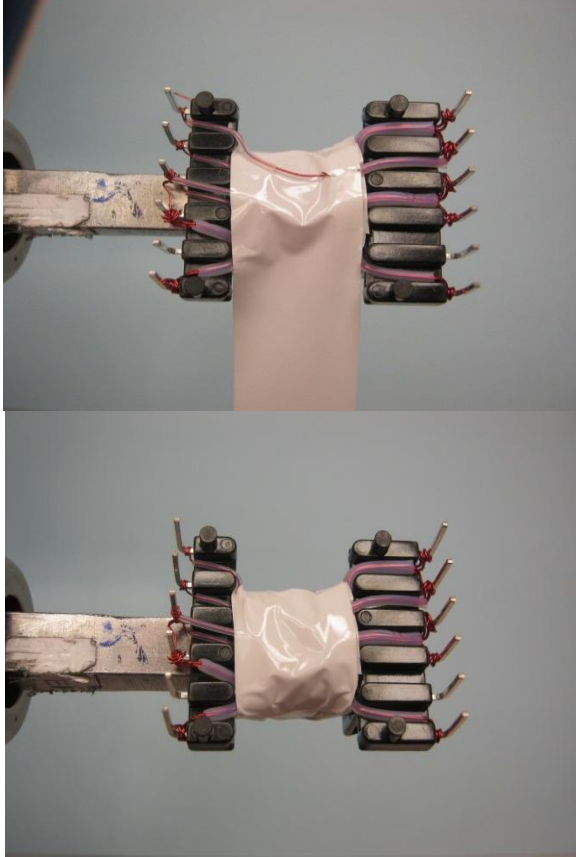
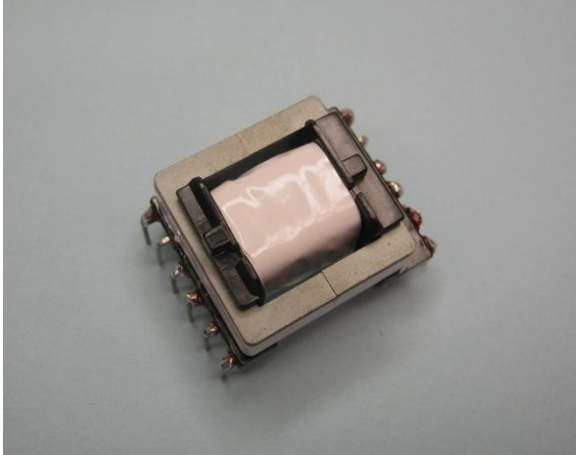
	 <p><i>return wires not overlap onto margin tape</i></p>	<p>At the last turn bring the wire back to the left, and terminate at pin 1.</p>
<p>Insulation</p>		<p>Place 3 layers of tape item [9].</p>
<p>WD3 1st Secondary</p>		<p>Start at pins 8, 7, wind 3 quad-filar turns of wire item [4] from right to left, spread the wire evenly,</p>



		<p>At the last turn bring the wire back to the right, and terminate at pin 10, 9.</p>
<p>Insulation</p>		<p>Place 1 layer of tape item [8].</p>
<p>WD4 2nd Secondary</p>		<p>Start at pins 12, wind 7 bi-filar turns of wire item [5] from right to left, spread the wire evenly,</p>

		<p>At the last turn bring the wire back to the right, and terminate at pin 8.</p>
<p>Insulation</p>		<p>Place 3 layers of tape item [9].</p>
<p>WD5 2nd Half Primary</p>		<p>Start at pin 4, wind 30 turns of wire item [3] from left to right with tight tension,</p>



		<p>At the last turn bring the wire back to the left, and terminate at pin 6.</p>
<p>Core Assembly</p>		<p>Grind and secure core halves with tape.</p>
<p>Varnish Transformer and Finish</p>		<p>Varnish item [10].</p>

9 效能資料

All measurements performed at room temperature and 50 Hz line frequency, except where otherwise stated. For all tests, the full load is 1000 mA for the 5 V output and 670 mA for the 18 V output (17 W total output power).

9.1 工作模式效率

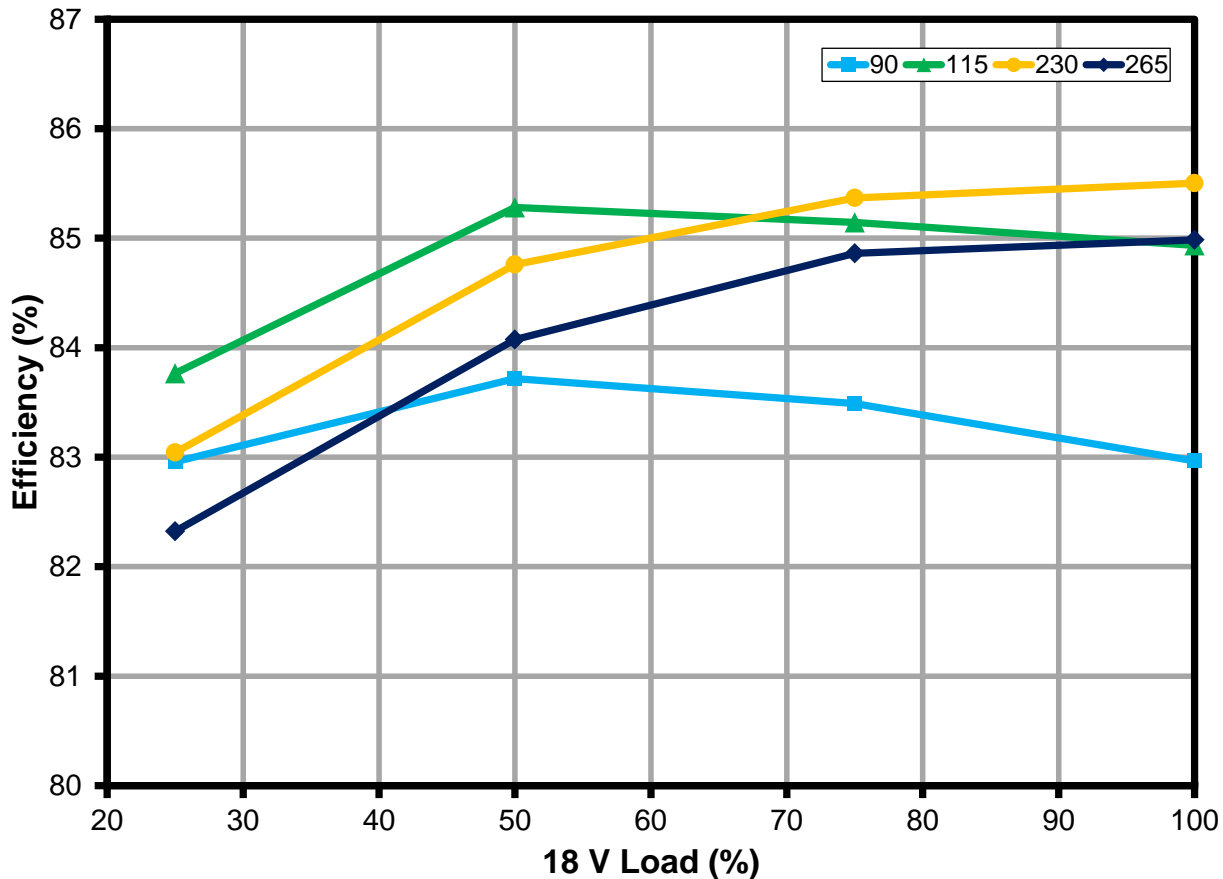


Figure 9 – Efficiency vs. LCD brightness, Room Temperature.



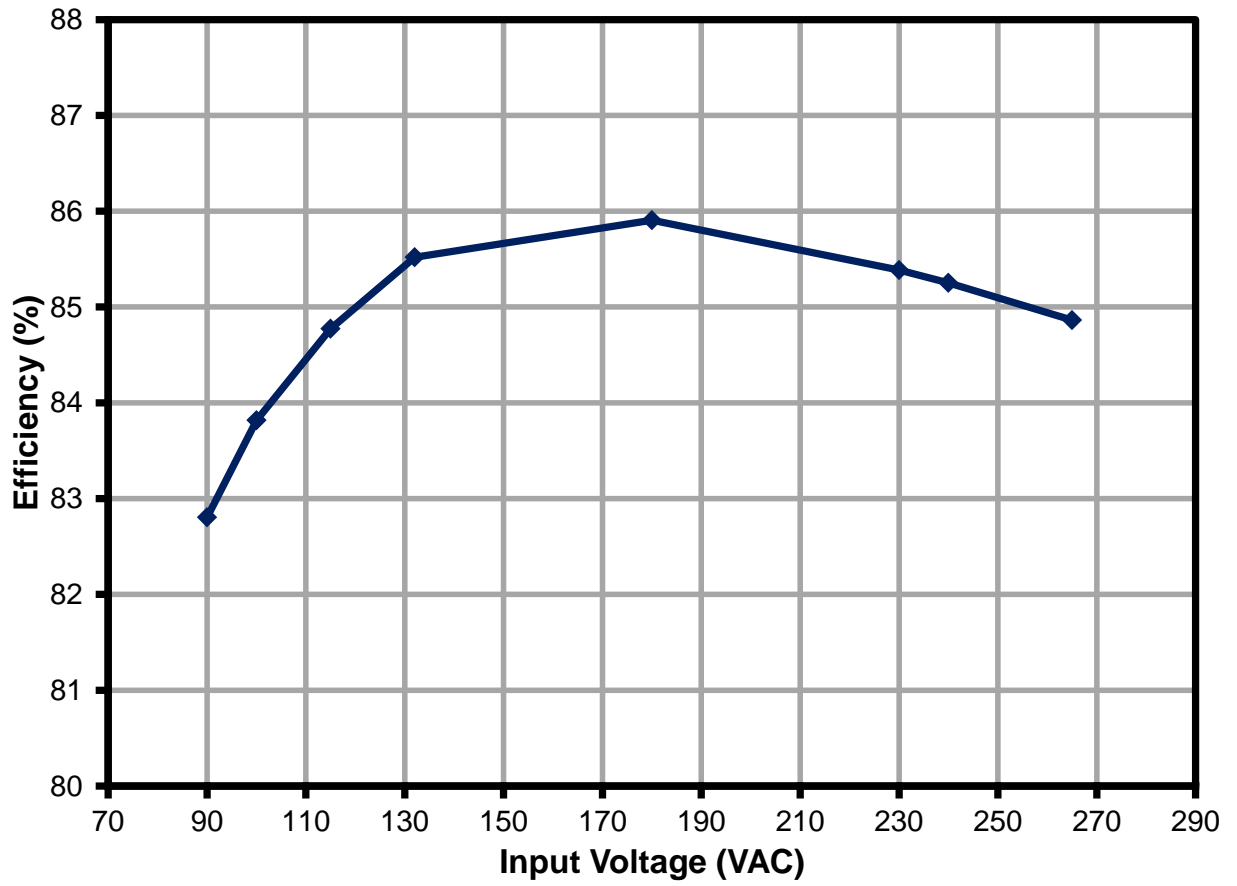


Figure 10 – Full Load Efficiency vs. Input Voltage, Room Temperature.

9.2 待機輸入功率和待機效率

Standby power and efficiency is measured using a 10 mA load on the 5 V output. The 18 V output is unloaded.

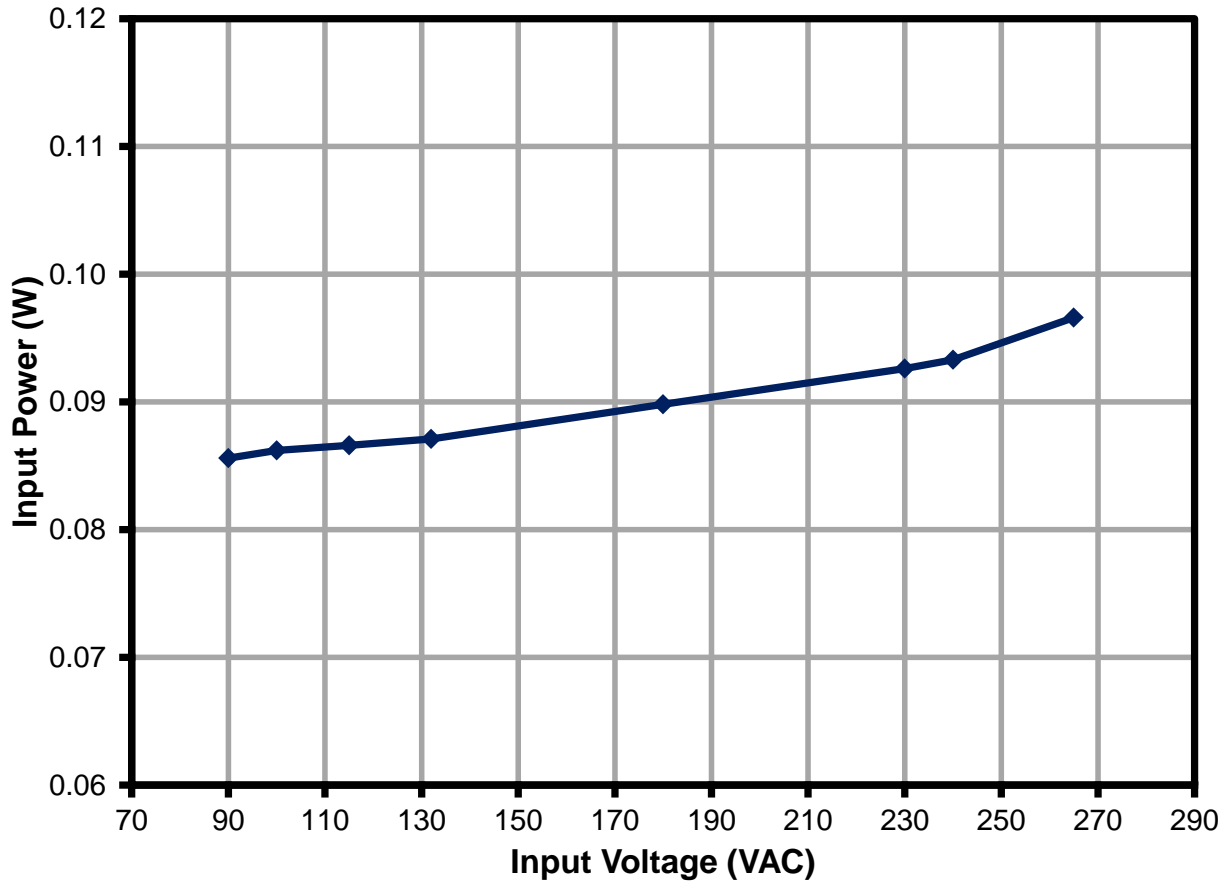


Figure 11 – Standby Input Power vs. Input Line Voltage, Room Temperature.



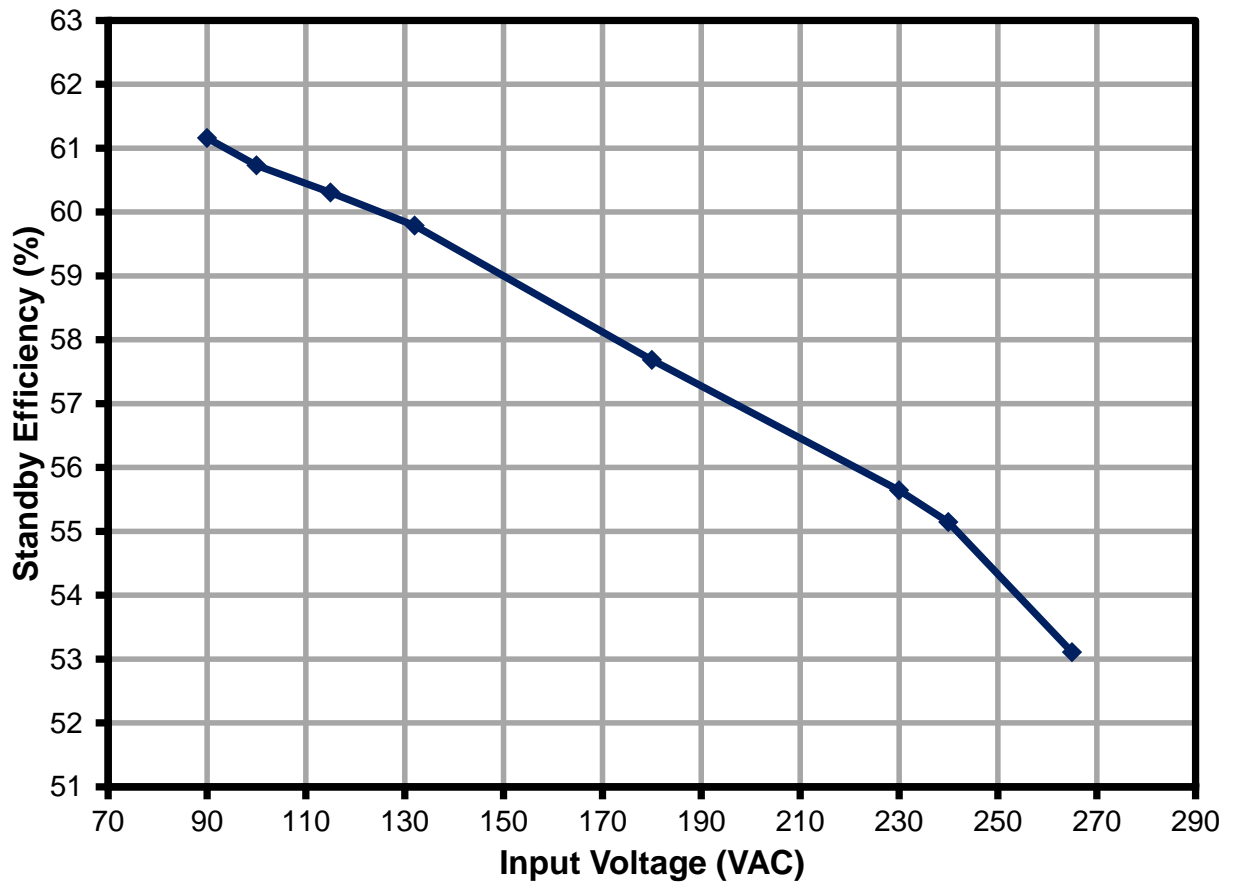


Figure 12 – Standby Efficiency vs. Input Voltage, Room Temperature.



9.3 在 18 V 0.67 A DC 負載和 5 V 1 A 平均負載條件下的線電壓調節

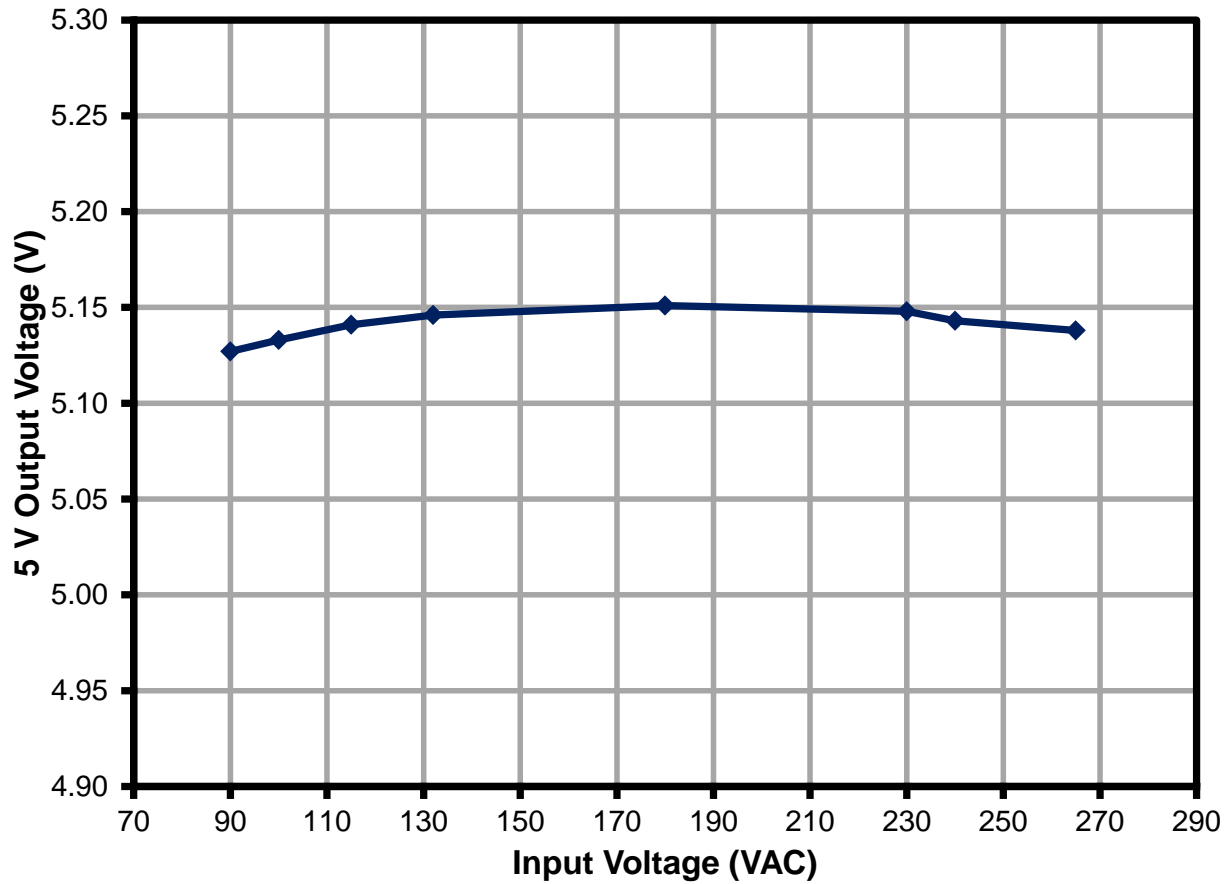


Figure 13 – 5 V Line Regulation under Full Load.



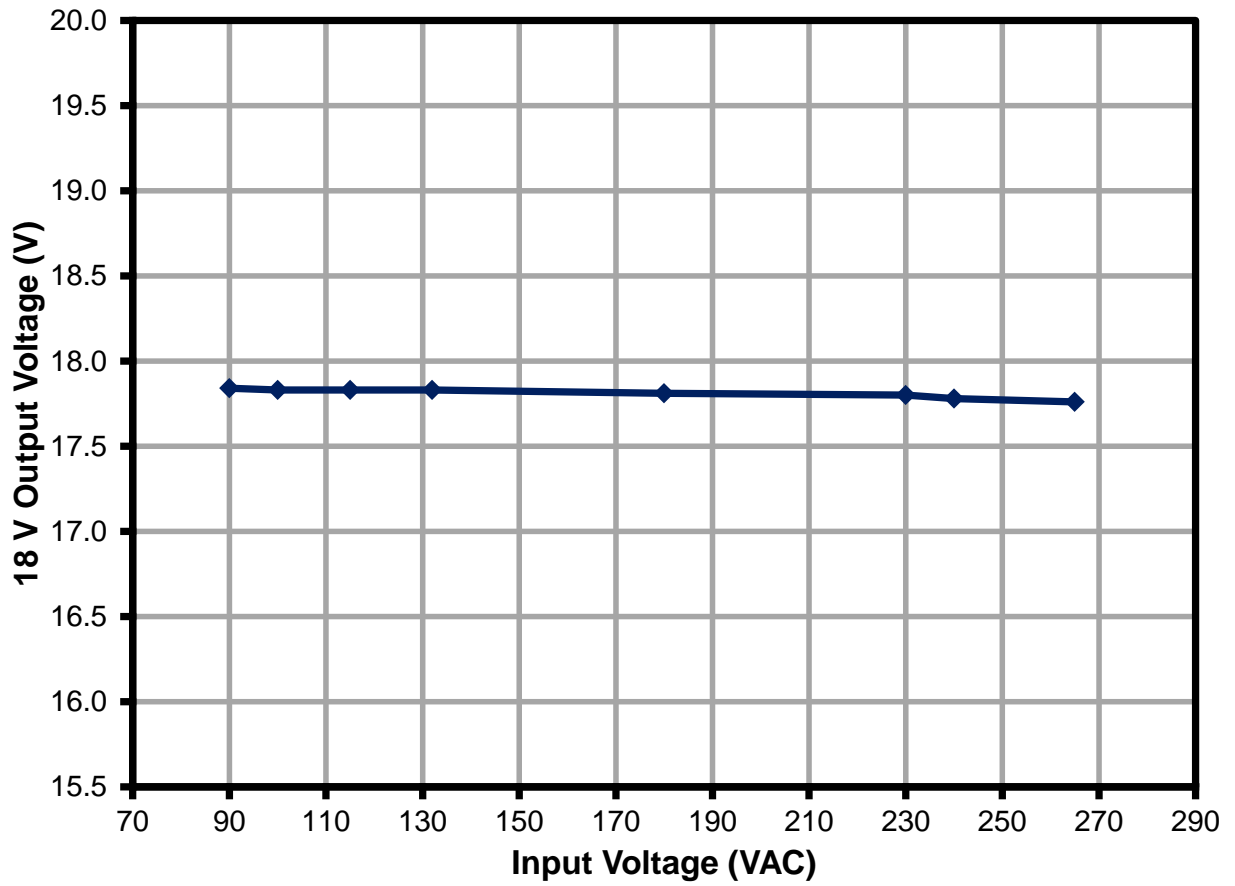


Figure 14 – 18 V Line Regulation under Full Load.



9.4 指定動態負載輪廓 (包括峰值、最小值和平均值) 下的輸出電壓

9.4.1 峰值和最小輸出電壓的測試方法

Figure 15 shows how the peak value and minimum value were collected. The power supply was loaded with the specified load profile in Figure 3. 18 V output load (LCD brightness) is always a pulsed load from 0 to 0.67 A with different duty cycle and 5 V load is always transient from 0.5 A to 1.5 A. Scope were used to record the peak value and minimum value for both output voltage, and the mean value is recorded with multimeter.

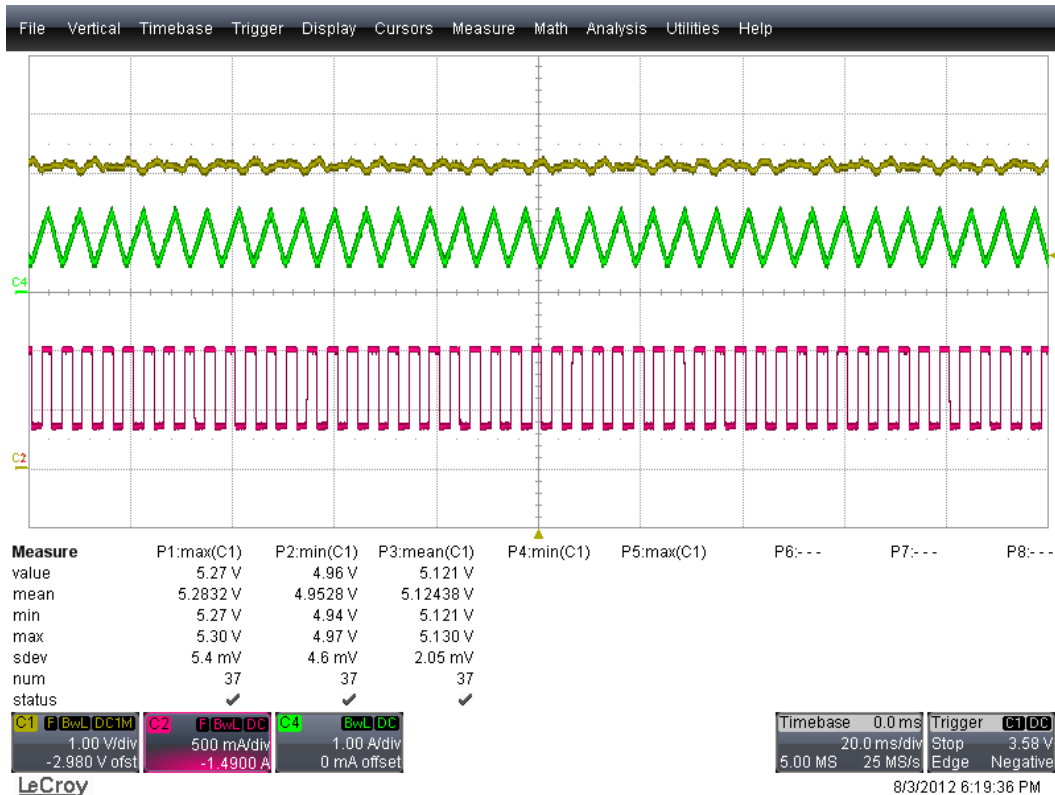


Figure 15 – Test Method for Peak and Minimum Output Voltage.



9.4.2 指定負載輪廓下的 5 V 輸出電壓

Figures below shows mean regulation (measured with multimeter), peak and minimum output voltage (measured with scope) under specified dynamic load profile.

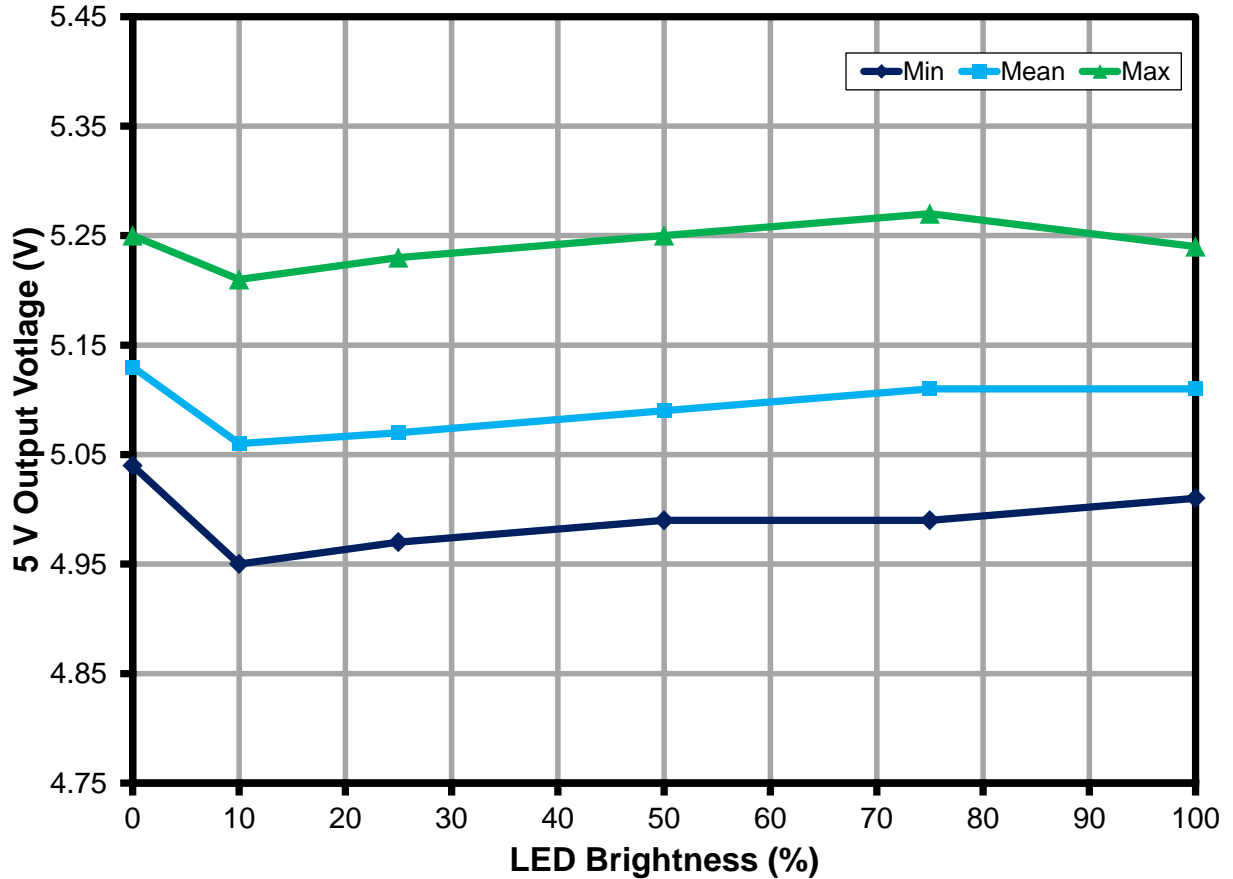


Figure 16 – 5 V Output Voltage under Specified Load Profile at 90 VAC.



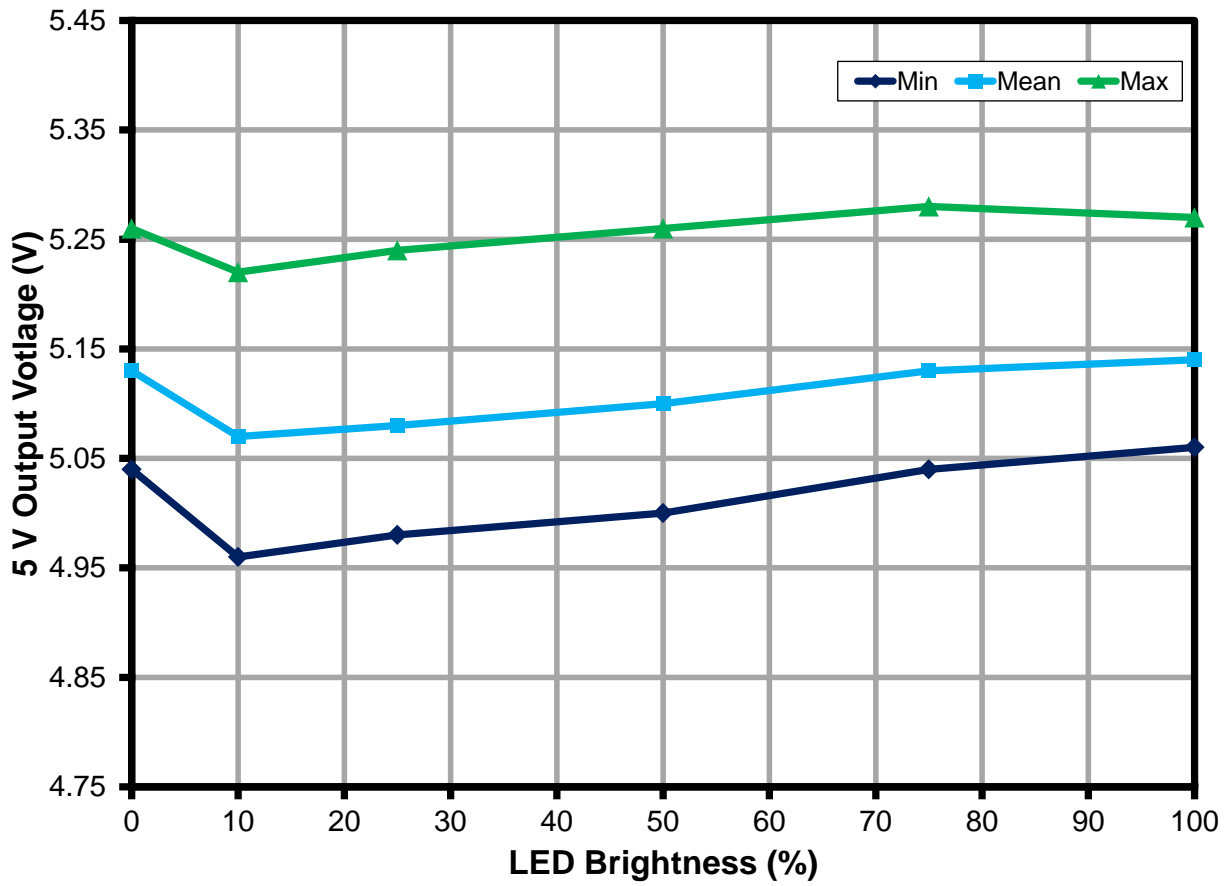


Figure 17 – 5 V Output Voltage under Specified Load Profile at 115 VAC.



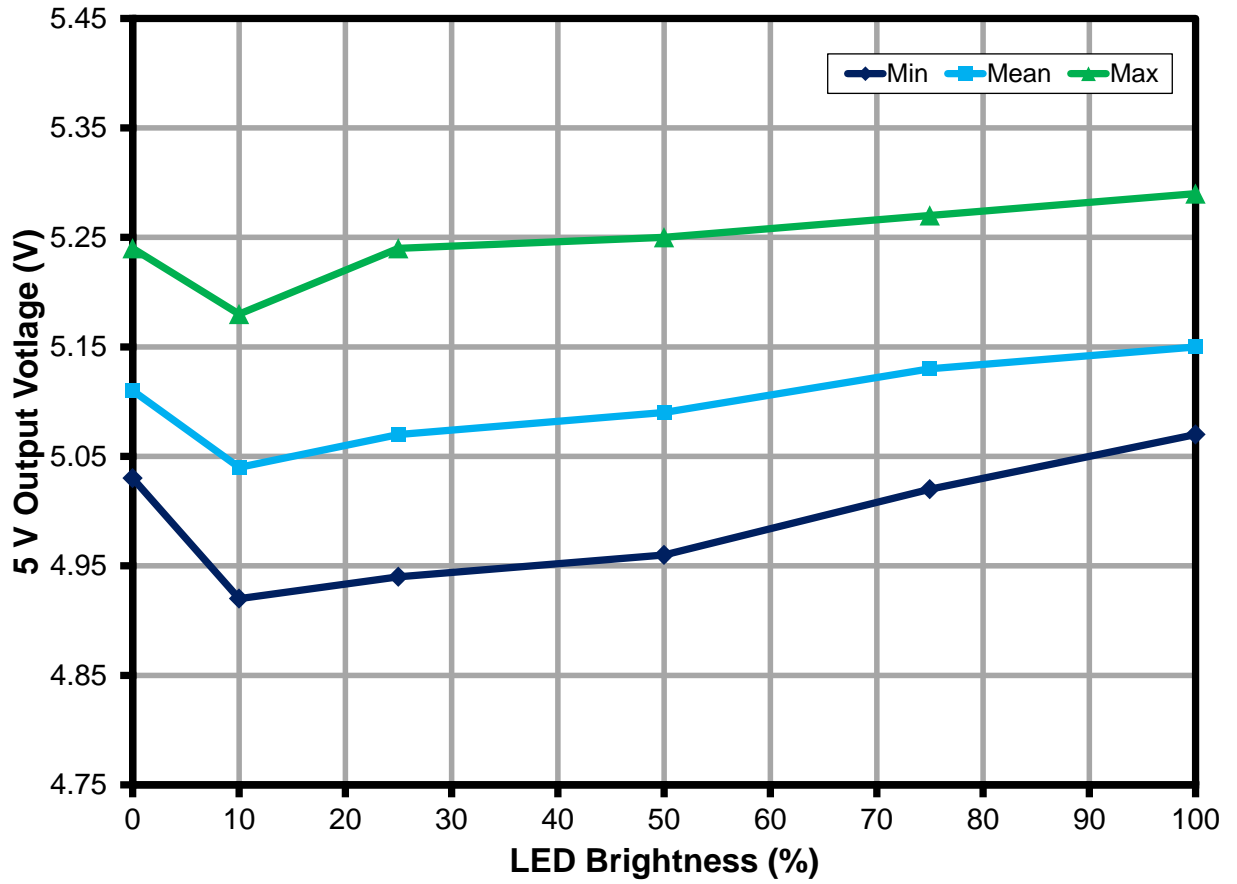


Figure 18 – 5 V Output Voltage under Specified Load Profile at 230 VAC.

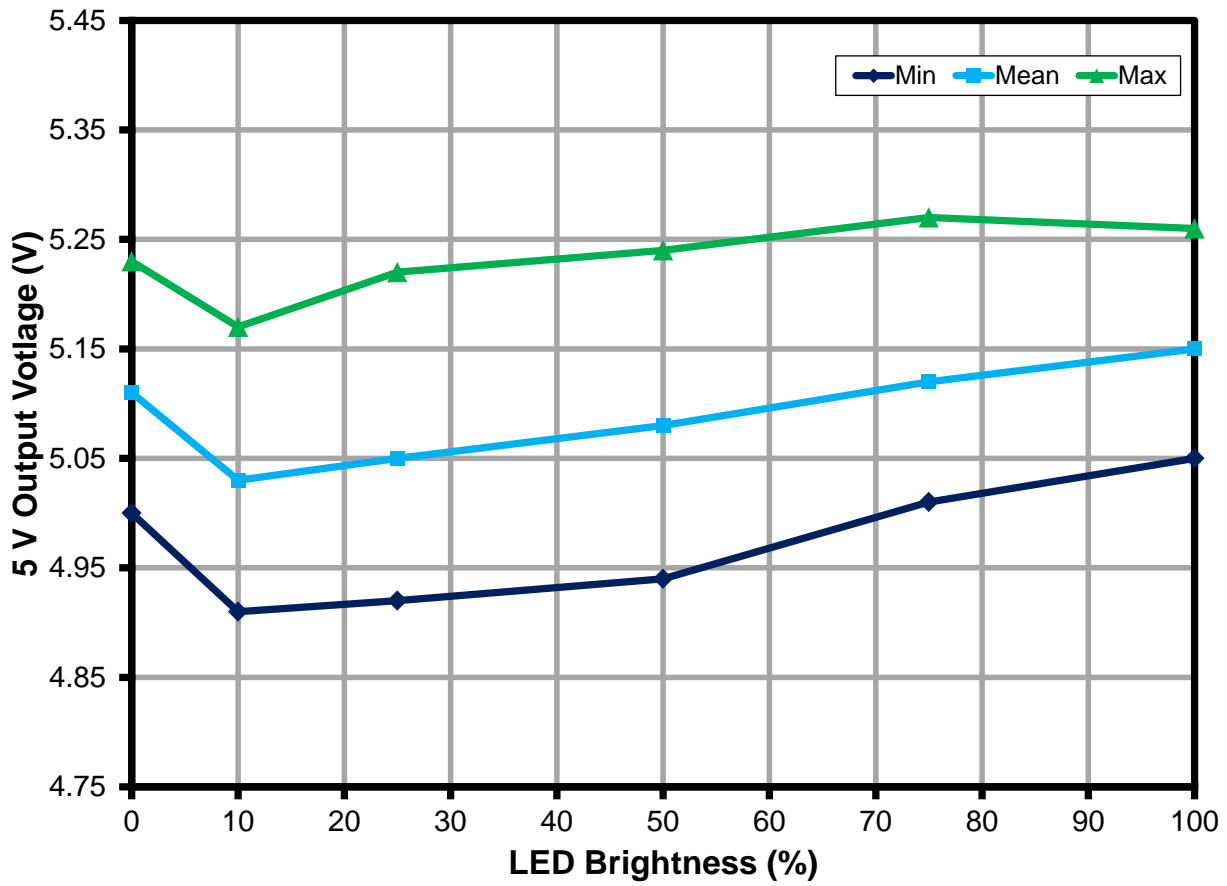


Figure 19 – 5 V Output Voltage under Specified Load Profile at 265 VAC.



9.4.3 指定負載配置下的 18 V 輸出電壓

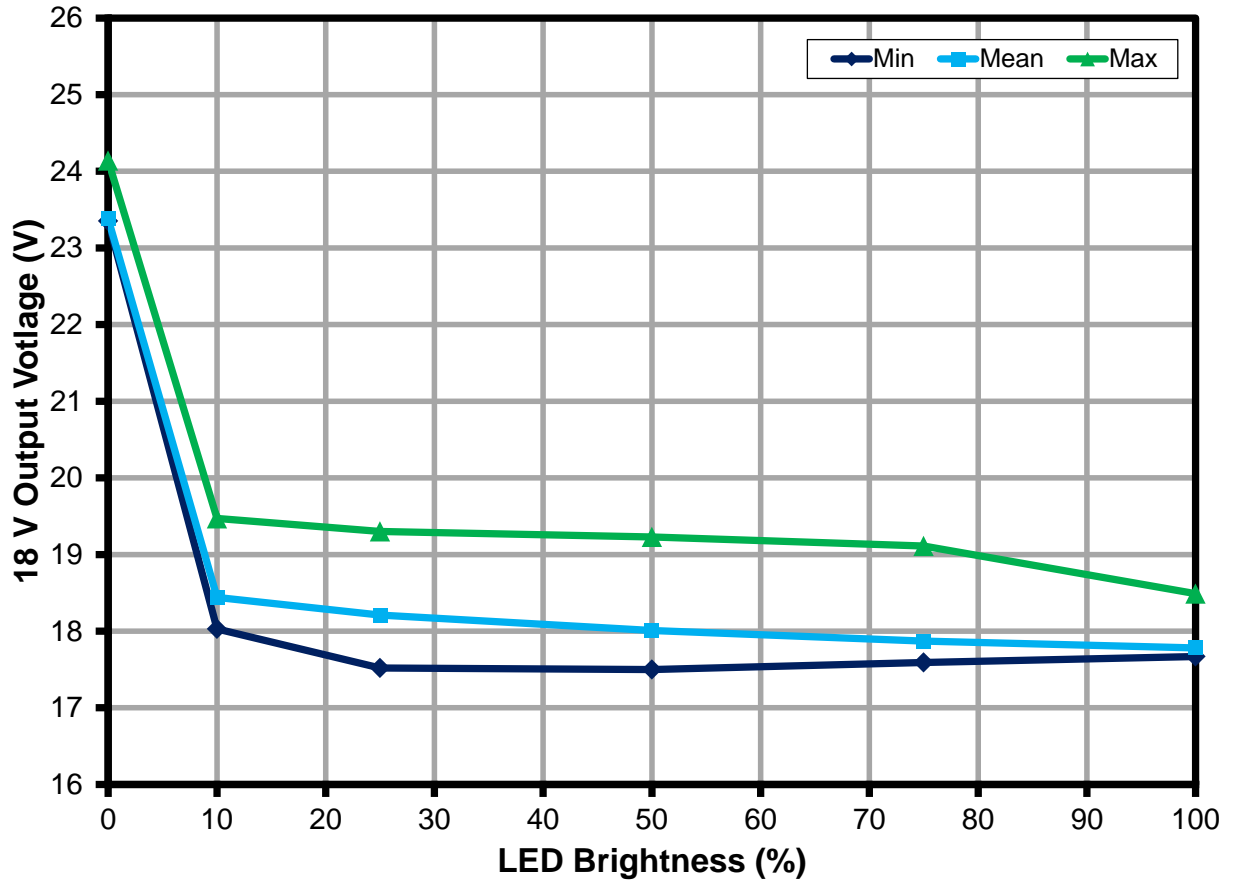


Figure 20 – 18 V Output Voltage under Specified Load Profile at 90 VAC

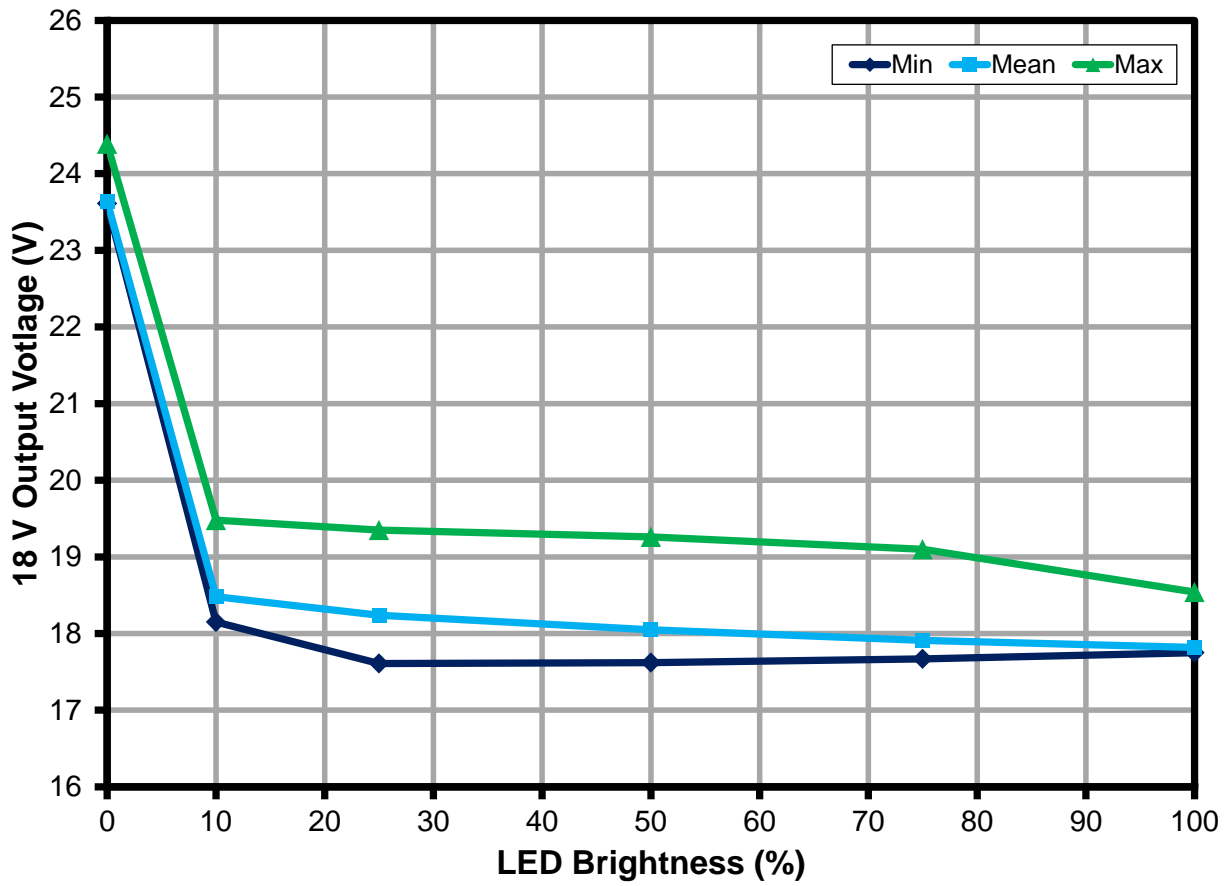


Figure 21 – 18 V Output Voltage under Specified Load Profile at 115 VAC.



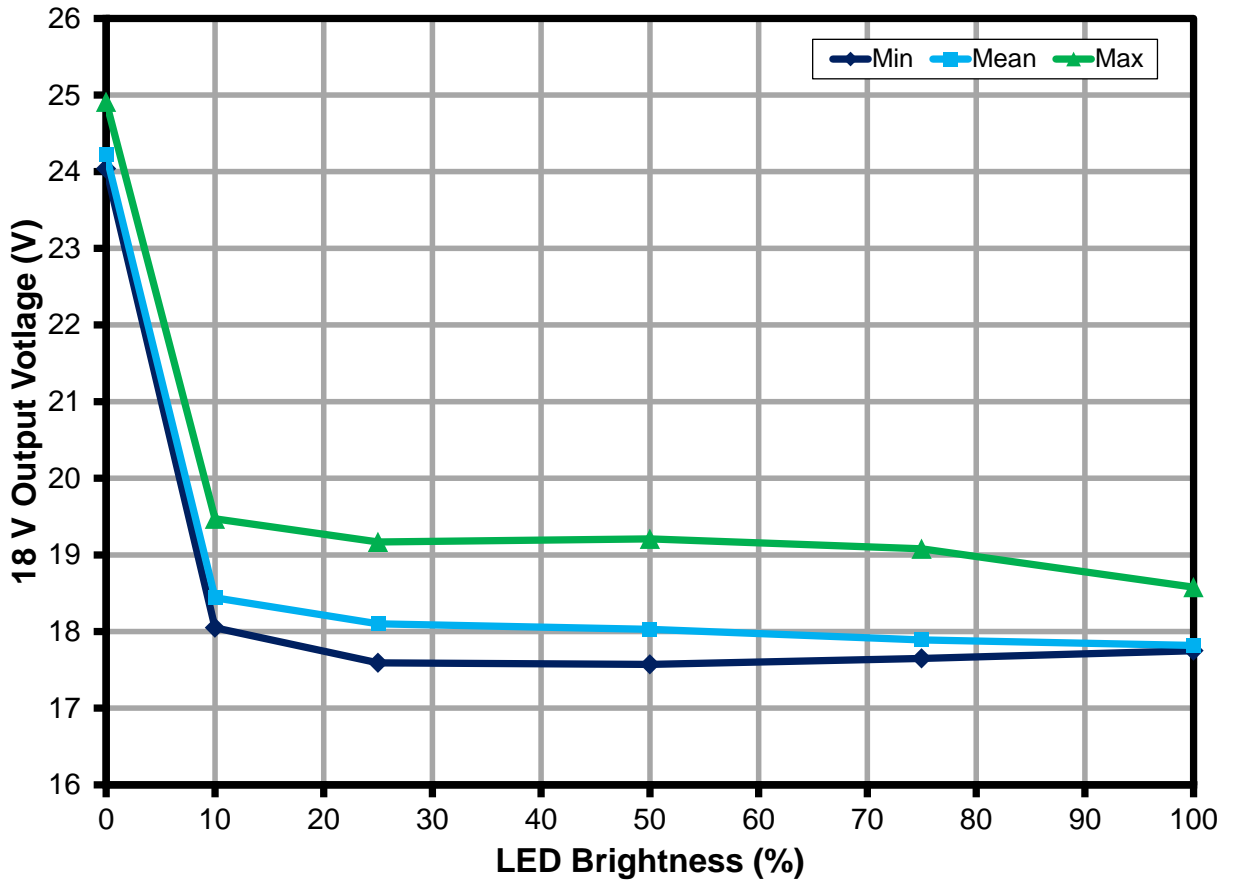


Figure 22 – 18 V Output Voltage under Specified Load Profile at 230 VAC.

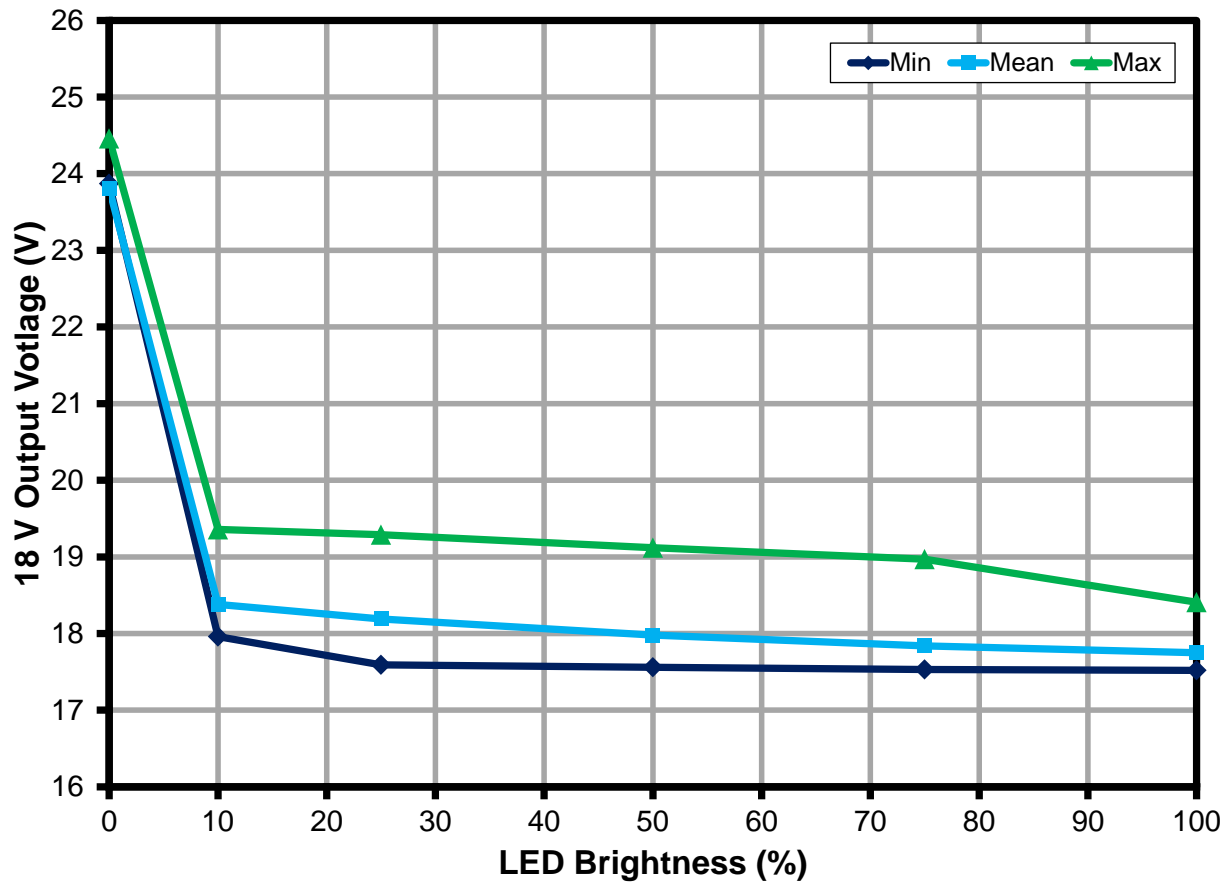


Figure 23 – 18 Output Voltage under Specified Load Profile at 265 VAC.



10 散熱效能

The unit was allowed to reach thermal equilibrium prior to the measurement. Figure 24 is the temperature profile of the board at room temperature.

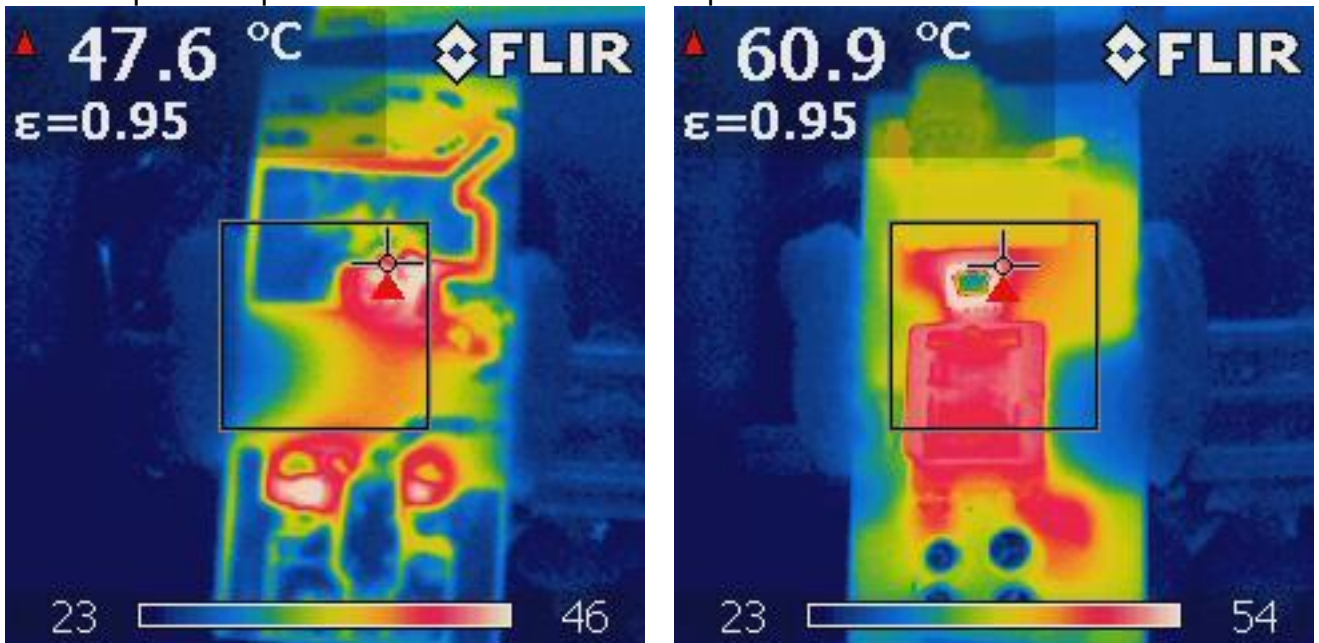


Figure 24 – Top (Right) and Bottom (left) Side Thermal Images at 265 VAC, Full Load, Room Temperature.

Table below shows the temperature of key components at 40 °C. The power supply was sealed into a box first, and the box was placed into a thermal chamber with 40 °C ambient. Temperatures of LinkSwitch-HP SOURCE pin and cathode pin of the output diode were measured at system full load (18 V/0.67 A, 5 V/1 A average). Temperature was recorded after the thermal reading was stable.

Temperature measurements of key components were taken using T-type (Copper-Constantan) thermocouples. The thermocouples were soldered directly to a SOURCE pin of the LNK6774V device and to the cathode of the output rectifier. The thermocouples were glued to the external core and to winding surfaces of the transformer.

The unit was sealed inside a large box to eliminate any air currents. The ambient temperature outside the box was raised to 40 °C. The unit was then operated at full load (5 V, 1 A and 18 V 0.67 A) and the temperature measurements were taken after they stabilized for 1 hour at 40 °C.



Temperature (°C)		
Item	90 VAC	265 VAC
LN6774V (U1)	76	79
5 V Output Diode	63	63
18 V Output Diode	61	61
Transformer	61	68

These results show that the IC has an acceptable rise in temperature.



11 波形

11.1 汲極電壓和電流，正常操作 on

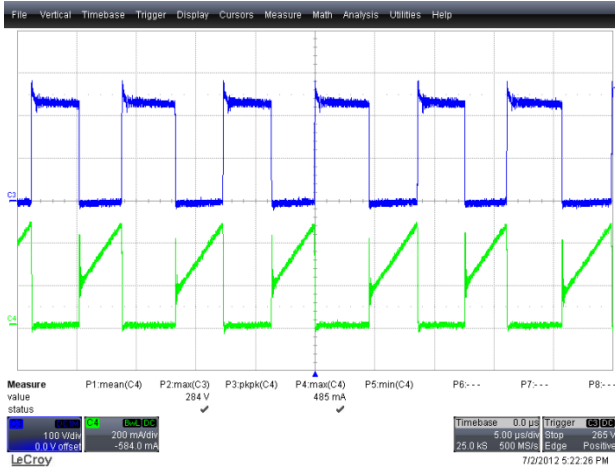


Figure 25 – 90 VAC, Full Load.
Upper: V_{DRAIN} , 100 V / div.
Lower: I_{DRAIN} , 0.2 A, 5 μ s / div.

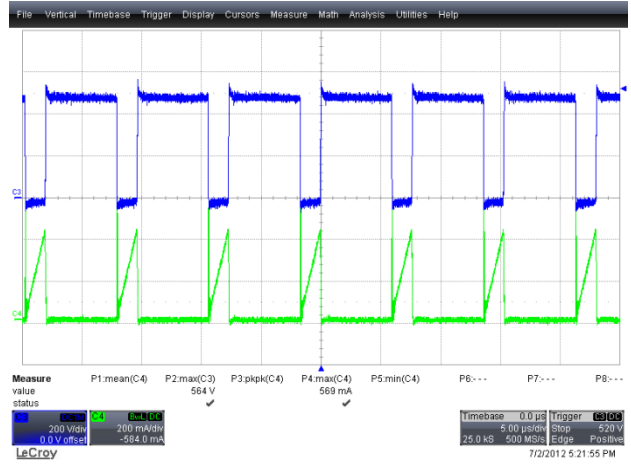


Figure 26 – 265 VAC, Full Load.
Upper: V_{DRAIN} , 200 V / div.
Lower: I_{DRAIN} , 0.2 A, 5 μ s / div.

11.2 汲極電壓和電流啟動配置

Drain and current profile during startup was tested with 5 V average 1 A load and 18 V no-load, since the power supply always start up into 18 V no load based on the specification. 5 V was tested with the dynamic load specified in the specification.

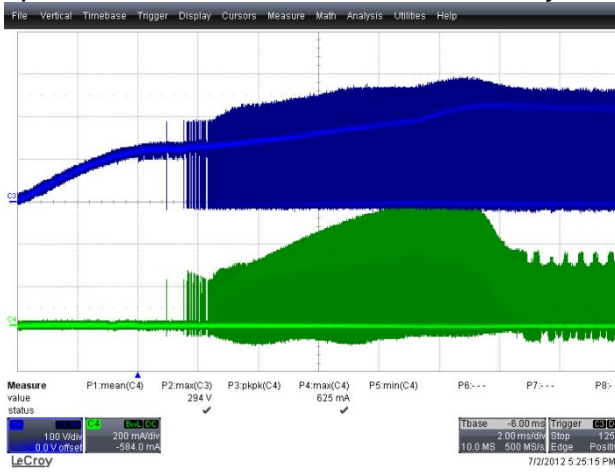


Figure 27 – 90 VAC, 5 V Dynamic, 18 V No-Load. Upper: V_{DRAIN} , 100 V / div.
Lower: I_{DRAIN} , 0.2 A, 2 ms / div.

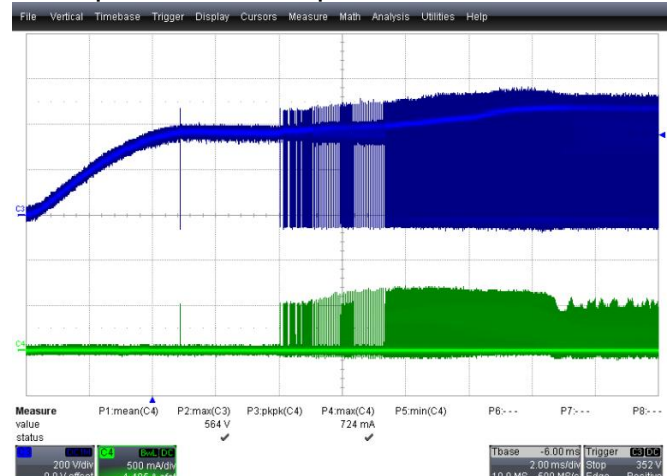


Figure 28 – 265 VAC 5 V Dynamic, 18 V No-Load.
Upper: V_{DRAIN} , 200 V / div.
Lower: I_{DRAIN} , 0.5 A, 2 ms / div.



11.3 書出電壓啟動配置 (含輸入電壓)

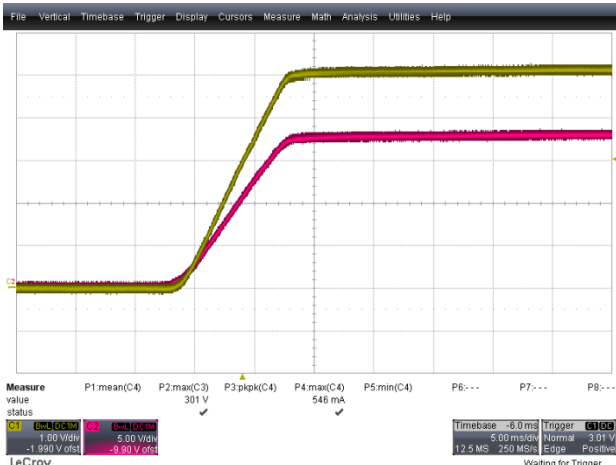


Figure 29 – Start-up Profile, 90 VAC, Standby Load.
 Upper: V_{OUT} , 5 V, 1 V / div.
 Lower: V_{OUT} , 18 V, 5 V, 5 ms / div.

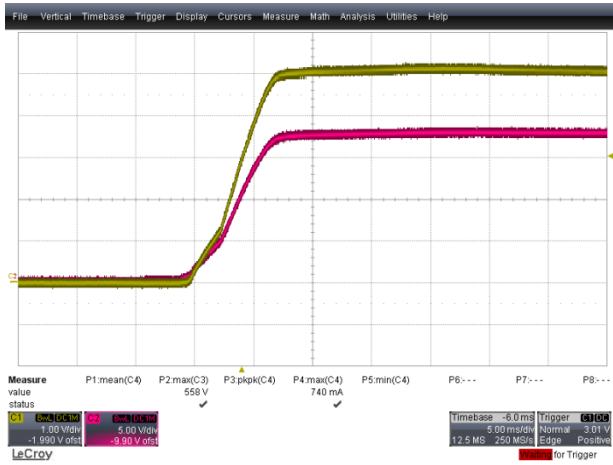


Figure 30 – Start-up Profile, 265 VAC, Standby Load.
 Upper: V_{OUT} , 5 V, 1 V / div.
 Lower: V_{OUT} , 18 V, 5 V, 5 ms / div.

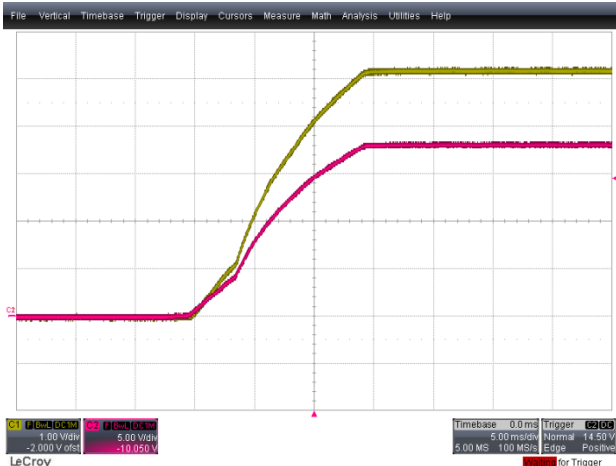


Figure 31 – Start-up Profile, 90 VAC, Full CC Load.
 Upper: V_{OUT} , 5 V, 1 V / div.
 Lower: V_{OUT} , 18 V, 5 V, 5 ms / div.

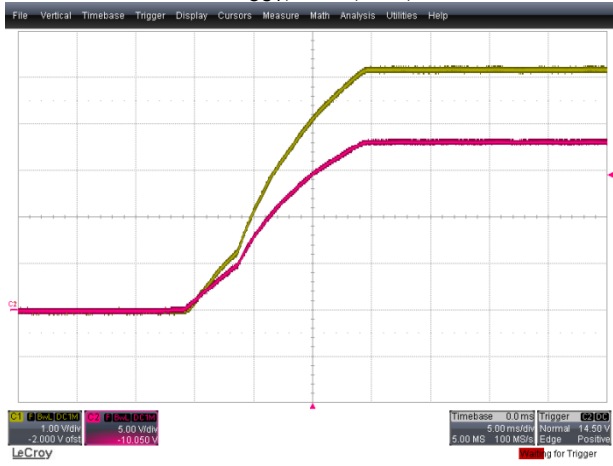


Figure 32 – Start-up Profile, 265 VAC, Full CC Load.
 Upper: V_{OUT} , 5 V, 1 V / div.
 Lower: V_{OUT} , 18 V, 5 V, 5 ms / div.

11.4 5 V 負載動態反應

11.4.1 使用 5 V 500 mA 至 1500 mA 步階負載和固定 18 V, 0.67 A DC 負載進行 5 V 動態測試

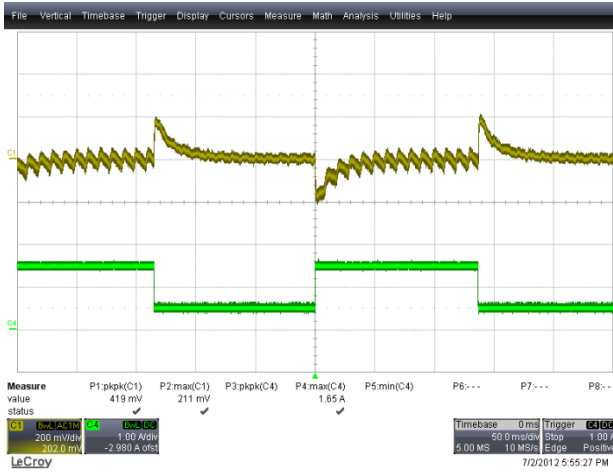


Figure 33 – 90 VAC, 18 V 0.67 A.
Upper: V_{OUT} , 5 V, 200 mV / div.
Lower: I_{OUT} , 5 V, 1 A, 50 ms / div.

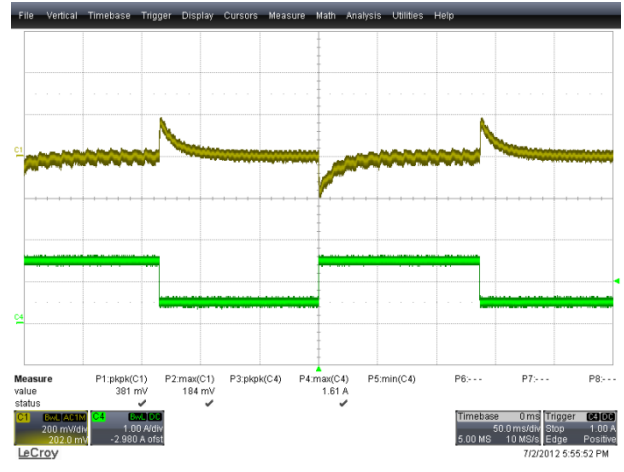


Figure 34 – 115 VAC, 18 V 0.67 A.
Upper: V_{OUT} , 5 V, 200 mV / div.
Lower: I_{OUT} , 5 V, 1 A, 50 ms / div.

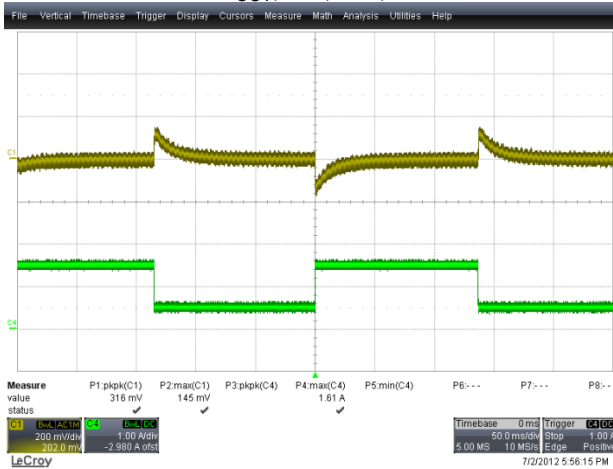


Figure 35 – 230 VAC, 18 V 0.67 A.
Upper: V_{OUT} , 5 V, 200 mV / div.
Lower: I_{OUT} , 5 V, 1 A, 50 ms / div.

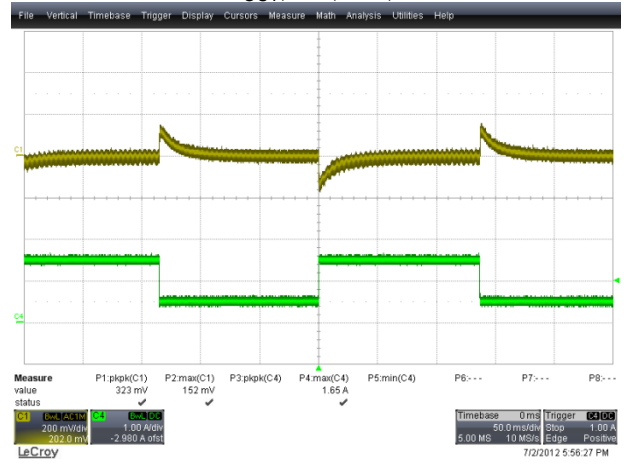


Figure 36 – 265 VAC, 18 V 0.67 A.
Upper: V_{OUT} , 5 V, 200 mV / div.
Lower: I_{OUT} , 5 V, 1 A, 50 ms / div.

11.4.2 使用指定負載配置的 5 V 動態測試

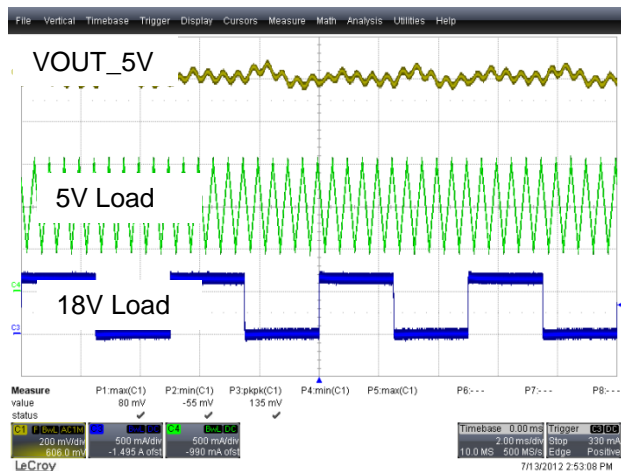


Figure 37 – 90 VAC, 5 V 1 A Dynamic Load and 18 V 0 to 0.67 A Step Load.
Upper: V_{OUT} , 5 V, 100 mV / div.
Lower: I_{OUT} , 18 V, 0.5 A, 5 ms / div.

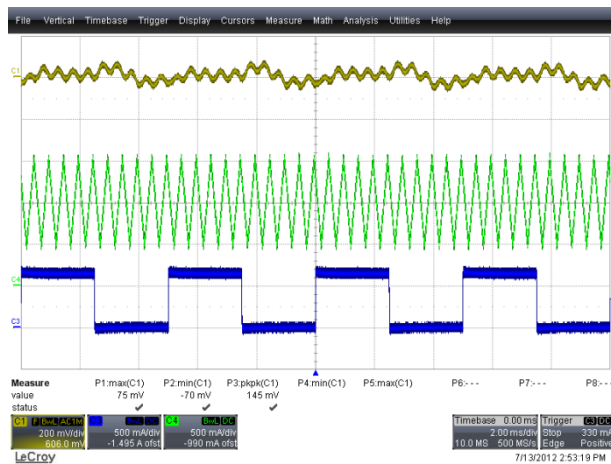


Figure 38 – 115 VAC, 5 V 1 A Dynamic Load and 18 V 0 to 0.67 A Step Load.
Upper: V_{OUT} , 5 V, 100 mV / div.
Lower: I_{OUT} , 18 V, 0.5 A, 5 ms / div.

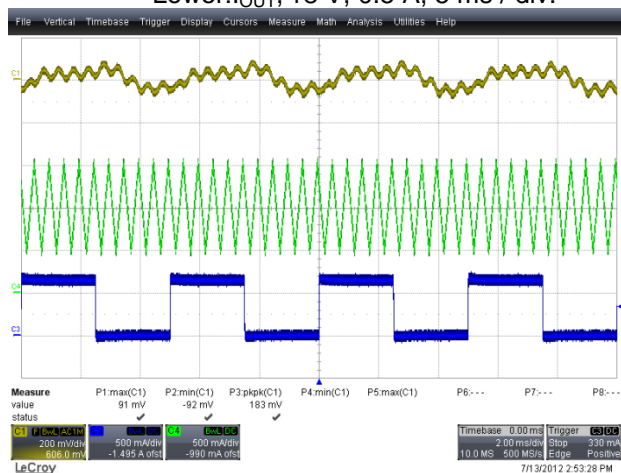


Figure 39 – 230 VAC, 5 V 1 A Dynamic Load and 18 V 0 to 0.67 A Step Load.
Upper: V_{OUT} , 5 V, 100 mV / div.
Lower: I_{OUT} , 18 V, 0.5 A, 5 ms / div.

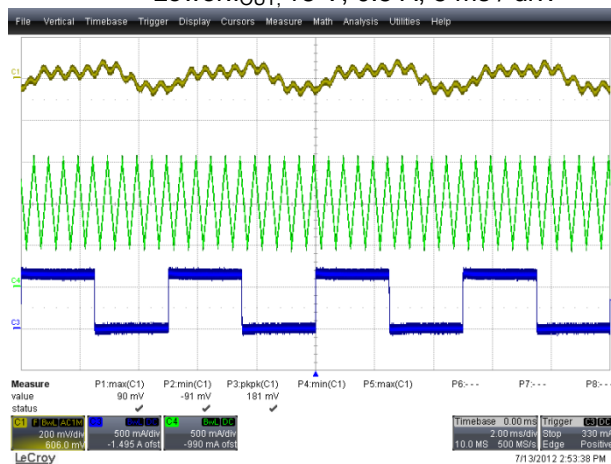


Figure 40 – 265 VAC, 5 V 1 A Dynamic Load and 18 V 0 to 0.6 A Step Load.
Upper: V_{OUT} , 5 V, 100 mV / div.
Lower: I_{OUT} , 18 V, 0.5 A, 5 ms / div.



11.4.3 使用指定負載配置的 18 V 動態測試

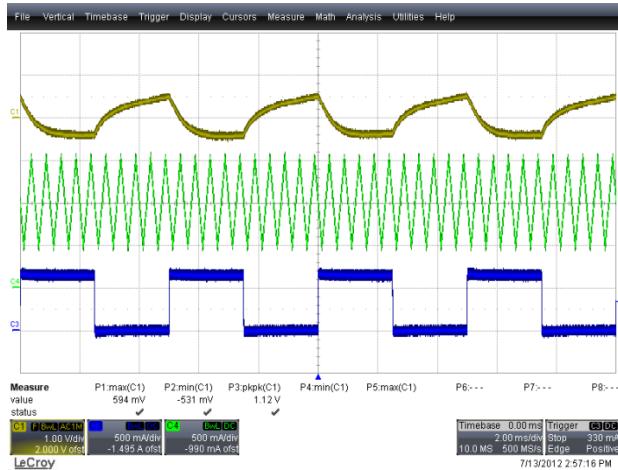


Figure 41 – 90 VAC, 5 V 1 A Average Load.
Upper: V_{OUT} , 18 V, 1 V / div.
Lower: I_{OUT} , 18 V, 0.5 A, 5 ms / div.

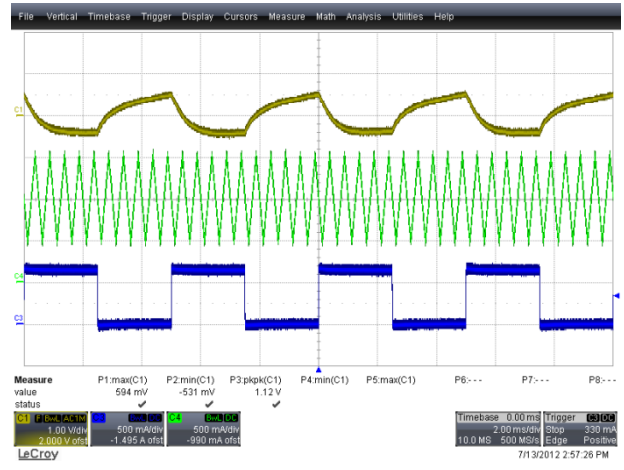


Figure 42 – 115 VAC, 5 V 1 A Average Load.
Upper: V_{OUT} , 18 V, 1 V / div.
Lower: I_{OUT} , 18 V, 0.5 A, 5 ms / div.

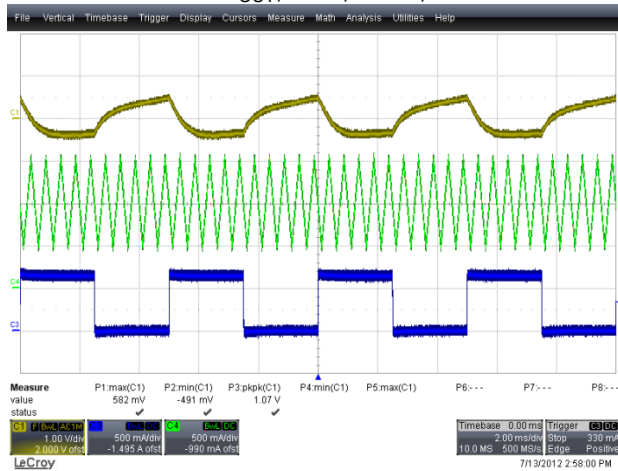


Figure 43 – 230 VAC, 5 V 1 A Average Load.
Upper: V_{OUT} , 18 V, 1 V / div.
Lower: I_{OUT} , 18 V, 0.5 A, 5 ms / div.

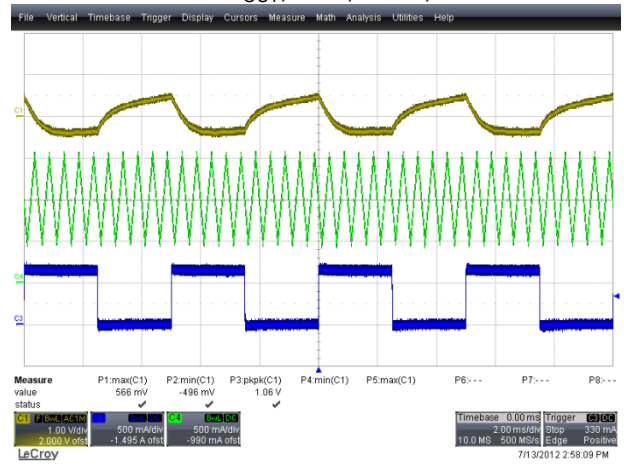


Figure 44 – 265 VAC, 5 V 1 A Average Load.
Upper: V_{OUT} , 18 V, 1 V / div.
Lower: I_{OUT} , 18 V, 0.5 A, 5 ms / div.

11.5 輸出漣波和雜訊測量

11.5.1 漣波測量技術

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the figures below.

The 5125BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF / 50 V ceramic type and one (1) 1.0 μF / 50 V aluminum electrolytic. **The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).**

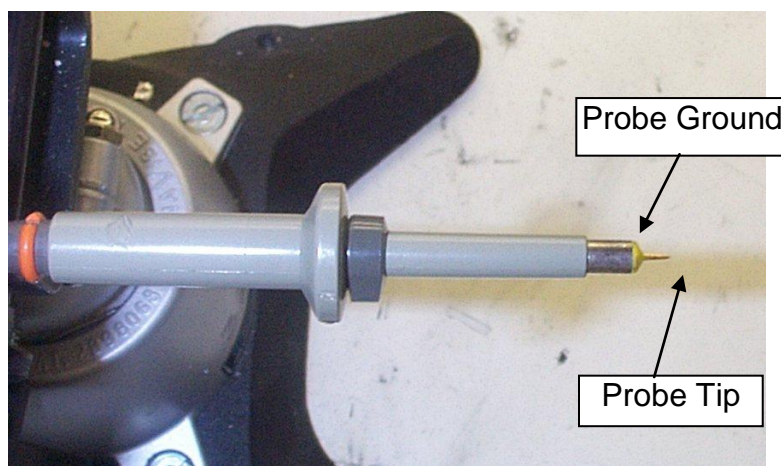


Figure 45 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed).

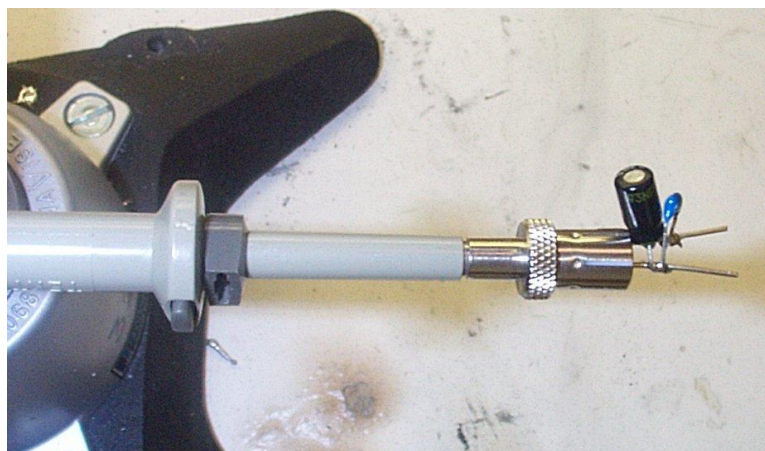


Figure 46 – Oscilloscope Probe with Probe Master 5125BA BNC Adapter. (Modified with wires for probe ground for ripple measurement, and two parallel decoupling capacitors added).

11.5.2 18 V 最大負載和 5 V 1 A 穩定負載下測試 18 V 的漣波

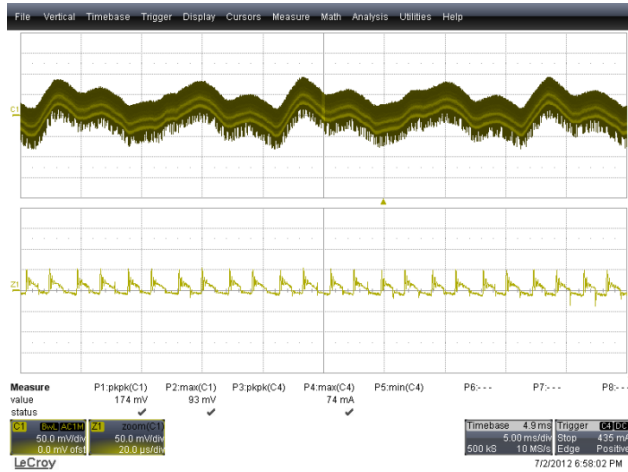


Figure 47 – 18 V Ripple, 90 VAC, Full Load.
 Upper: 18 V_{RIPPLE}, 5 ms, 50 mV / div.
 Lower: 18 V_{RIPPLE}, 20 μs, 50 mV / div.

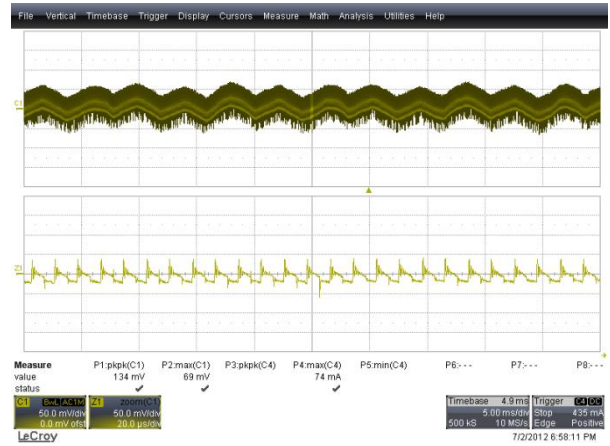


Figure 48 – 18 V Ripple, 115 VAC, Full Load.
 Upper: 18 V_{RIPPLE}, 5 ms, 50 mV / div.
 Lower: 18 V_{RIPPLE}, 20 μs, 50 mV / div.

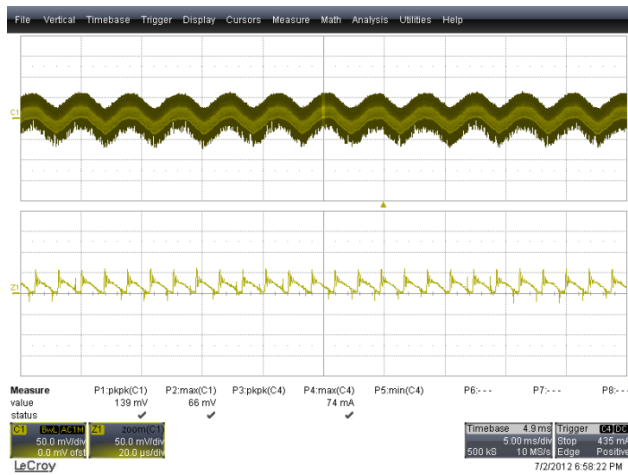


Figure 49 – 18 V_{RIPPLE}, 230 VAC, Full Load.
 Upper: 18 V_{RIPPLE}, 5 ms, 50 mV / div.
 Lower: 18 V_{RIPPLE}, 20 μs, 50 mV / div.

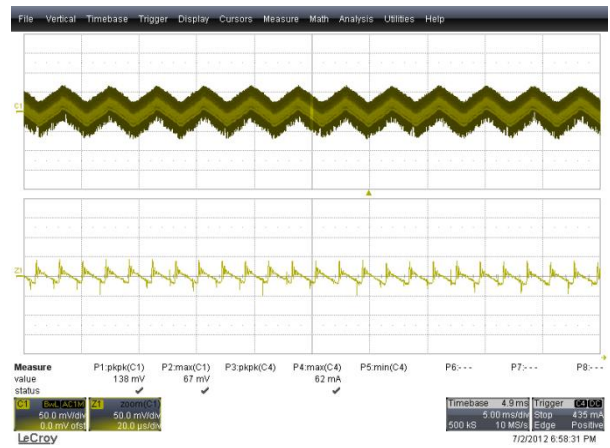


Figure 50 – 18 V_{RIPPLE}, 265 VAC, Full Load.
 Upper: 18 V_{RIPPLE}, 5 ms, 50 mV / div.
 Lower: 18 V_{RIPPLE}, 20 μs, 50 mV / div.

11.5.3 18 最大負載和 5 V 1 A 穩定負載下測試 5 V 的漣波

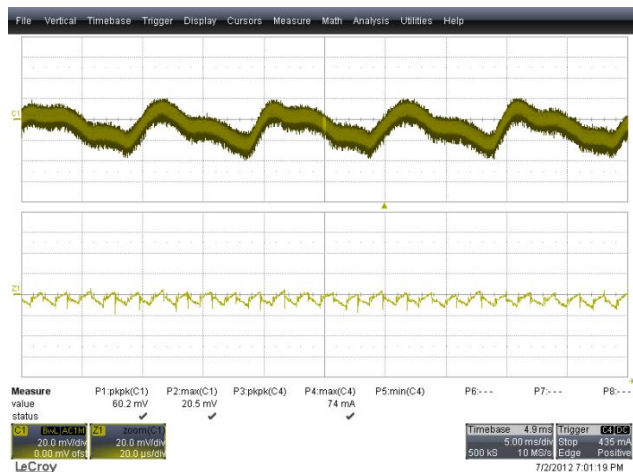


Figure 51 – Output Ripple, 90 VAC, Full Load.
 Upper: $5 V_{RIPPLE}$, 5 ms, 20 mV / div.
 Lower: $5 V_{RIPPLE}$, 20 μ s, 20 mV / div.

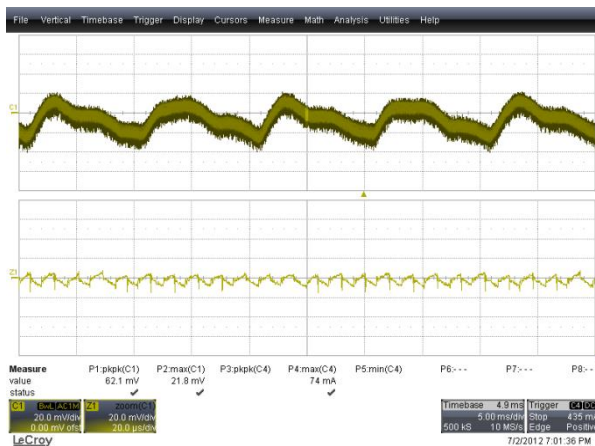


Figure 52 – Output Ripple, 115 VAC, Full Load.
 Upper: $5 V_{RIPPLE}$, 5 ms, 20 mV / div.
 Lower: $5 V_{RIPPLE}$, 20 μ s, 20 mV / div.

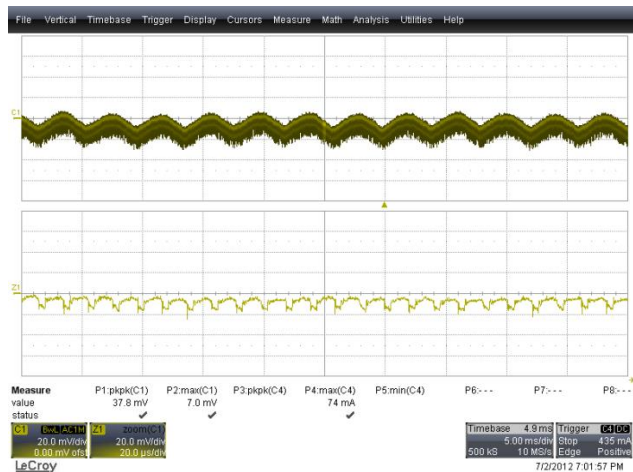


Figure 53 – Output Ripple, 230 VAC, Full Load.
 Upper: $5 V_{RIPPLE}$, 5 ms, 20 mV / div.
 Lower: $5 V_{RIPPLE}$, 20 μ s, 20 mV / div.

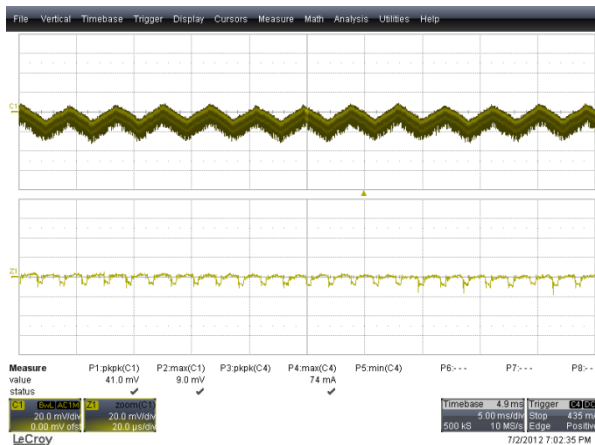


Figure 54 – Output Ripple, 265 VAC, Full Load.
 Upper: $5 V_{RIPPLE}$, 5 ms, 20 mV / div.
 Lower: $5 V_{RIPPLE}$, 20 μ s, 20 mV / div.



12 保護功能

12.1 短路自動重新啓動

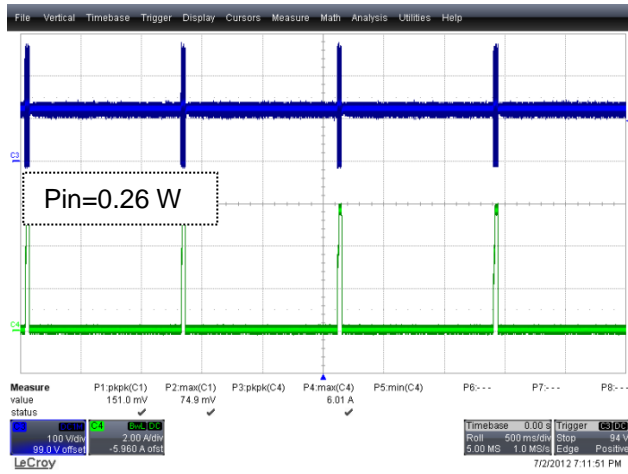


Figure 55 – Short-Circuit, 90 VAC.
Upper: V_{DS} , 100 V / div.
Lower: $5 V_{LOAD}$, 500 ms, 2 A / div.

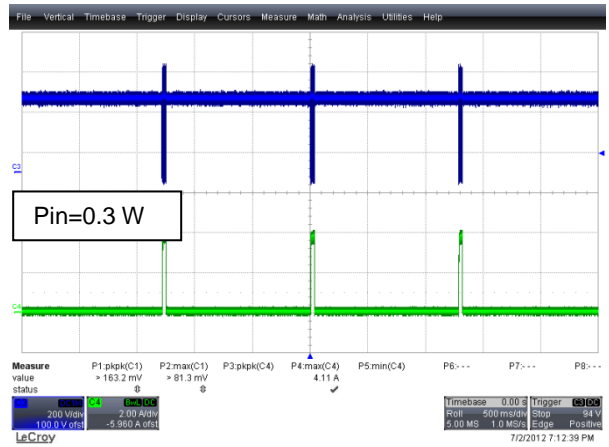


Figure 56 – Short-Circuit, 265 VAC.
Upper: V_{DS} , 200 V / div.
Lower: $5 V_{LOAD}$, 500 ms, 2 A / div.

12.2 輸出過壓保護

Output OVP was tested by connecting a 100 kΩ resistor between CP pin and BP pin output.



Figure 57 – Output OVP, 265 VAC, Standby Load.
 V_{OUT} , 5 V, 1 V, 500 ms / div.

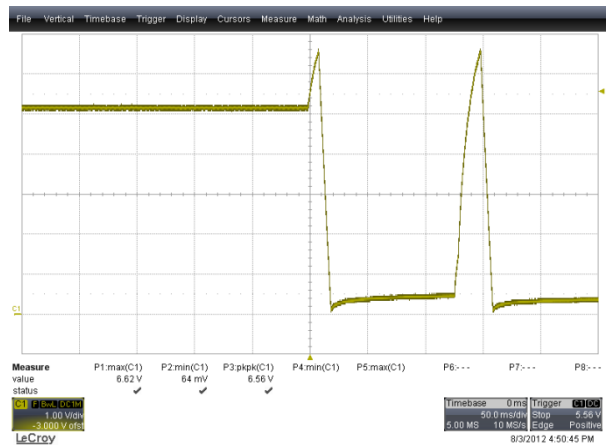


Figure 58 – Output OVP, 265 VAC, Full Load.
 V_{OUT} , 5 V, 1 V, 50 ms / div.



12.3 電壓啟動和電壓關閉測試

At full load, AC input was transient from 0 VAC to 120 VAC for brown-in test and from 120 VAC to 0 VAC for brown-out test. Slew rate of input voltage is 12 VAC/S for brown-in and brown-out test.

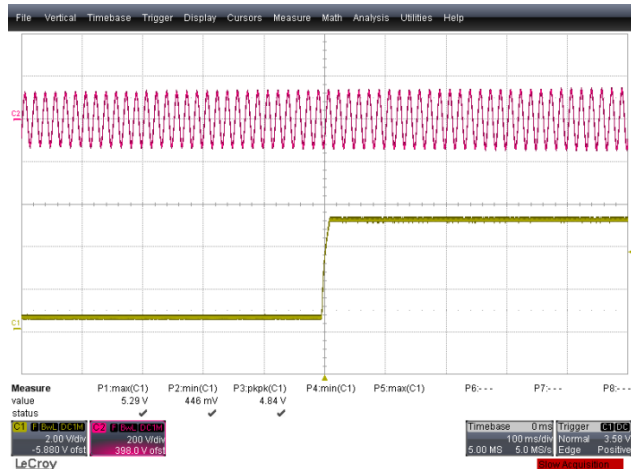


Figure 59 – Brown-In Test, Full Load.
 Upper: VAC, 200 V / div.
 Lower: 5 V_{OUT}, 2 V, 100 ms / div.

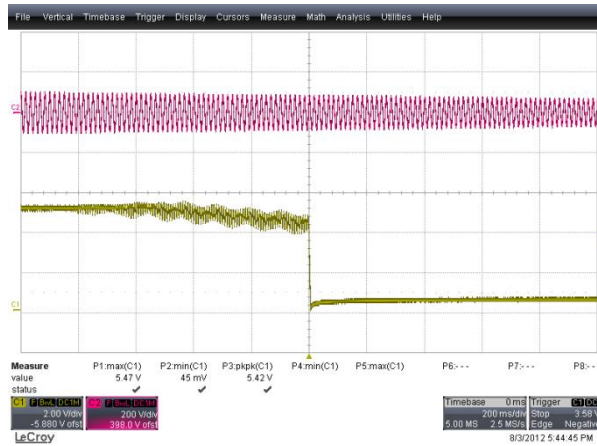


Figure 60 – Brown-In Test, Full Load.
 Upper: VAC, 200 V / div.
 Lower: 5 V_{OUT}, 2 V, 200 ms / div.

13 線電壓突波

Differential input line 1.2/50 μ s surge testing was conducted on a single test unit to IEC61000-4-5. Input voltage was set at 230 VAC. Resistor loads were used for both outputs (5 V/1 A and 18 V/0.67 A). Output regulation was verified after the test.

Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Results (Pass/Fail # Strikes)
D.M.		(2Ω source)		10 Strikes each Level
+1000	230	L1 to L2	90	Pass
-1000	230	L1 to L2	270	Pass
C.M.		(12Ω source)		
+2000	230	L1, L2 to PE	90	Pass
-2000	230	L1, L2 to PE	270	Pass

14 ESD

ESD passes at 8 kV for contact discharge and 15kV for air discharge, no output glitch and latch off was found during the test.

Device	Discharge Type	Discharge Location	Voltage	# of Events (1/sec)	Remarks
LNK6774V	Contact	+ Output Terminal	+8 kV	10	PASS
			-8 kV	10	PASS
		- Output Terminal	+8 kV	10	PASS
			-8 kV	10	PASS
	Air	+ Output Terminal	+15 kV	10	PASS
			-15 kV	10	PASS
		- Output Terminal	+15 kV	10	PASS
			-15 kV	10	PASS



15 滿載時的 EMI 測試

At 115 VAC and 230 VAC, conducted emissions tests were performed at full load (0.67A DC load for 18 V and 1 A DC load for 5 V). Composite EN55022B / CISPR22B conducted limits are shown. All the tests show excellent EMI performance.

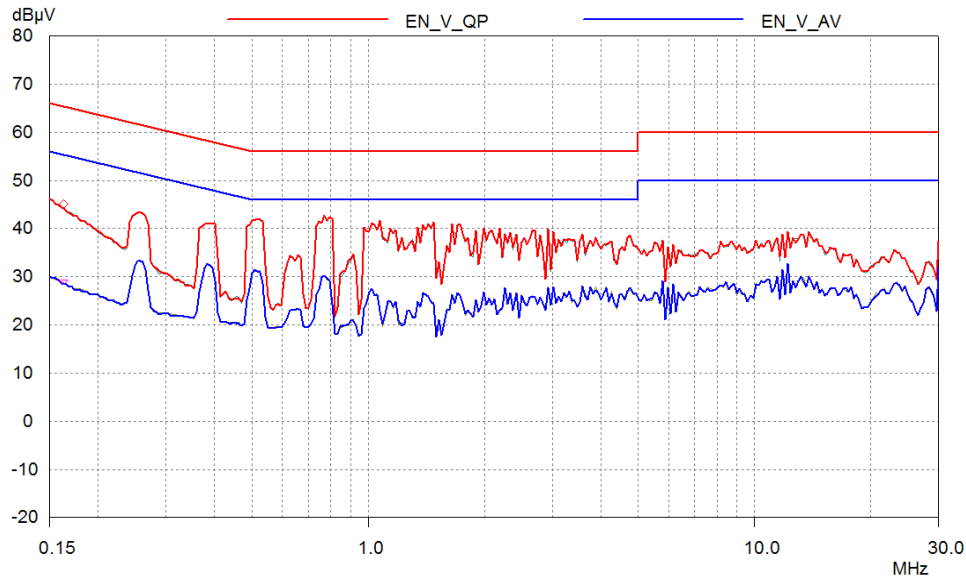


Figure 61 – Conducted EMI at 115 VAC 60 Hz, Full Load, Output Return Connected to Ground.

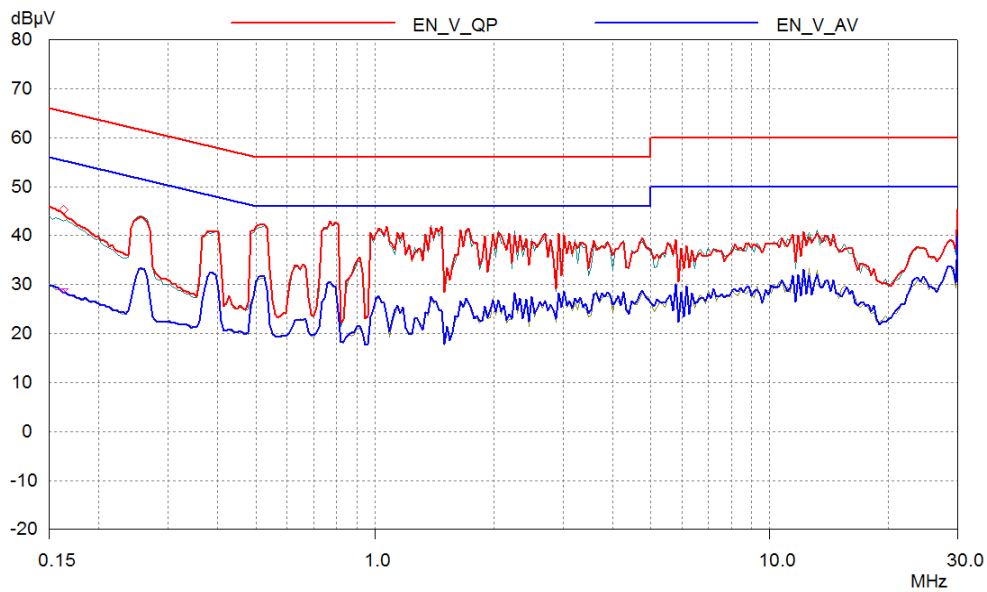


Figure 62 – Conducted EMI at 115 VAC 60 Hz, Full Load, Output Return Connected to Artificial Hand.



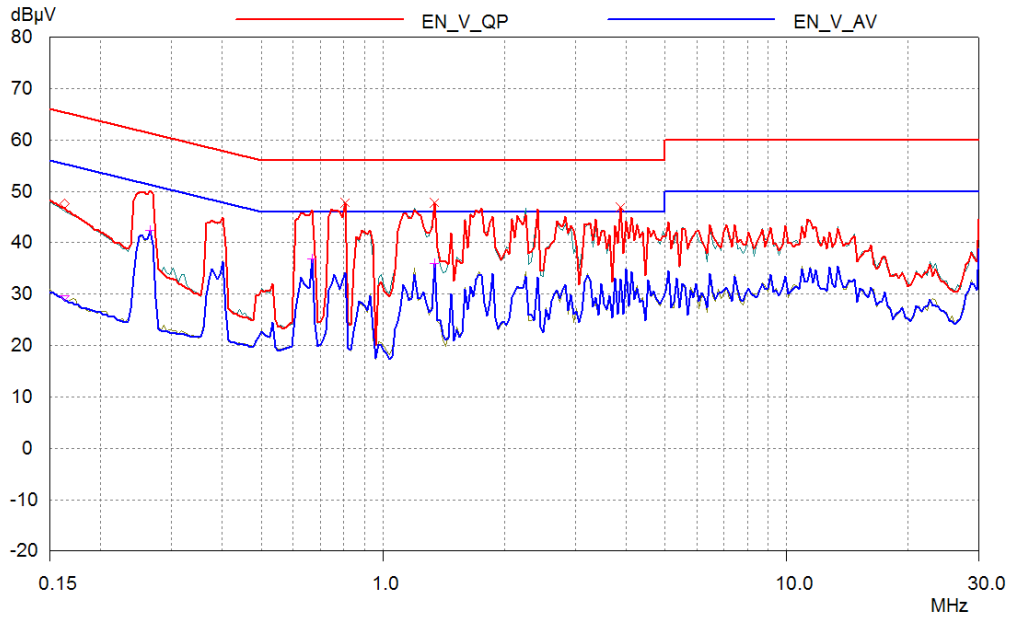


Figure 63 – Conducted EMI at 230 VAC 60 Hz, Full Load, Output Return Connected to Ground.

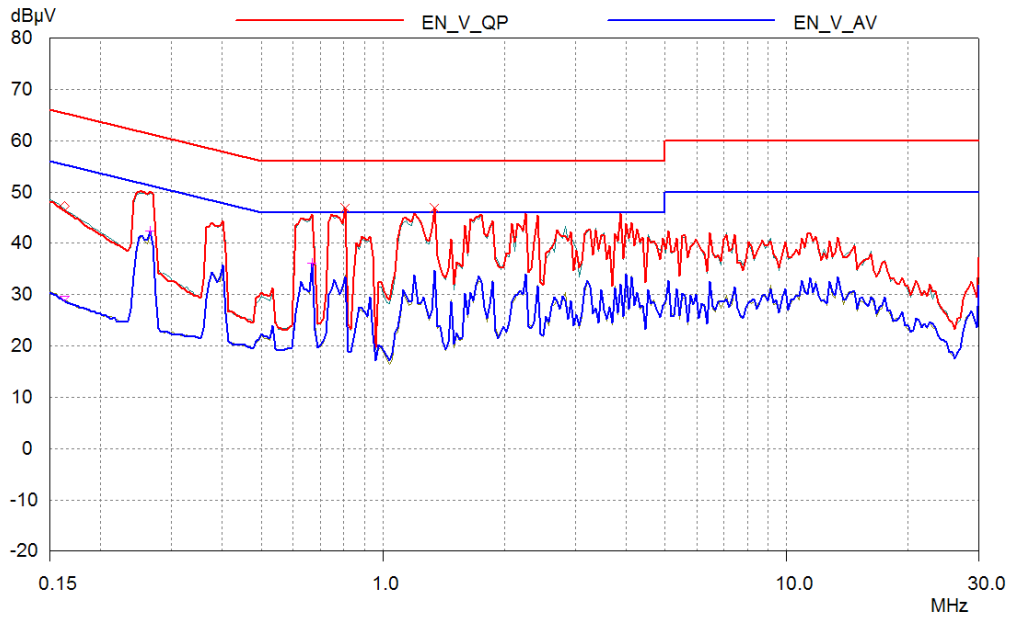


Figure 64 – Conducted EMI at 230 VAC 60 Hz, Full Load, Output Return Connected to Artificial Hand.



16 修訂記錄

Date	Author	Revision	Description & changes	Reviewed
28-Sep-12	KM	2.2	Initial Release	Marketing and Apps



如需最新更新，請造訪我們的網站：www.powerint.com

Power Integrations 保留隨時更改產品以提高可靠性或可製造性的權利。Power Integrations 對因使用此處所說明的任何裝置或電路所造成的損失概不負責。POWER INTEGRATIONS 在此不作任何保證，並明確否認所有保證，包括但不限於適售性、針對特定用途的適用性以及不侵犯第三方權利等默示保證。

專利資訊

本處所述的產品和應用 (包括 PI 裝置 IC 之外的變壓器結構和電路) 可能包含 Power Integrations 的一項或多項美國及國外專利，或是正在申請的美國及國外專利。www.powerint.com 上提供了 Power Integrations 專利的完整清單。Power Integrations 授予其客戶某些特定專利權的授權，詳情請參閱 <<http://www.powerint.com/ip.htm>>。

PI 標誌、TOPSwitch、TinySwitch、LinkSwitch、LYTSwitch、DPA-Switch、PeakSwitch、CAPZero、SENZero、LinkZero、HiperPFS、HiperTFS、HiperLCS、Qspeed、EcoSmart、Clamless、E-Shield、Filterfuse、StackFET、PI Expert 和 PI FACTS 均為 Power Integrations, Inc. 的商標。其他商標為其個別公司之財產。©Copyright 2013 Power Integrations, Inc.

Power Integrations 全球銷售支援地點

全球總部

5245 Hellyer Avenue
San Jose, CA 95138, USA.
總機：+1-408-414-9200
客戶服務：
電話：+1-408-414-9665
傳真：+1-408-414-9765
電子郵件：usasales@powerint.com

德國

Lindwurmstrasse 114
80337, Munich
Germany
電話：+49-895-527-39110
傳真：+49-895-527-39200
電子郵件：eurosales@powerint.com

日本

Kosei Dai-3 Building
2-12-11, Shin-Yokohama,
Kohoku-ku, Yokohama-shi,
Kanagawa 222-0033
Japan
電話：+81-45-471-1021
傳真：+81-45-471-3717
電子郵件：japansales@powerint.com

台灣

5F, No. 318, Nei Hu Rd.,
Sec. 1
Nei Hu District
Taipei 11493, Taiwan R.O.C.
電話：+886-2-2659-4570
傳真：+886-2-2659-4550
電子郵件：taiwansales@powerint.com

中國 (上海)

Rm 1601/1610, Tower 1,
Kerry Everbright City
No. 218 Tianmu Road West,
Shanghai, P.R.C. 200070
電話：+86-21-6354-6323
傳真：+86-21-6354-6325
電子郵件：chinasales@powerint.com

印度

#1, 14th Main Road
Vasanthanagar
Bangalore-560052
India
電話：+91-80-4113-8020
傳真：+91-80-4113-8023
電子郵件：indiasales@powerint.com

韓國

RM 602, 6FL
Korea City Air Terminal B/D,
159-6
Samsung-Dong, Kangnam-Gu,
Seoul, 135-728 Korea
電話：+82-2-2016-6610
傳真：+82-2-2016-6630
電子郵件：koreasales@powerint.com

歐洲總部

1st Floor, St. James's House
East Street, Farnham
Surrey GU9 7TJ
United Kingdom
電話：+44 (0) 1252-730-141
傳真：+44 (0) 1252-727-689
電子郵件：eurosales@powerint.com

中國 (深圳)

3rd Floor, Block A,
Zhongtuo International Business
Center, No. 1061, Xiang Mei Rd,
FuTian District, ShenZhen,
China, 518040
電話：+86-755-8379-3243
傳真：+86-755-8379-5828
電子郵件：chinasales@powerint.com

義大利

Via Milanese 20, 3rd.Fl.
20099 Sesto San Giovanni
(MI) Italy
電話：+39-024-550-8701
傳真：+39-028-928-6009
電子郵件：eurosales@powerint.com

新加坡

51 Newton Road,
#19-01/05 Goldhill Plaza
Singapore, 308900
電話：+65-6358-2160
傳真：+65-6358-2015
電子郵件：singaporesales@powerint.com

應用服務專線

全球 +1-408-414-9660

應用服務傳真

全球 +1-408-414-9760

