Design Example Report

Title	*10 W, 7.5 V Output Automotive Power Supply for 800 V Systems Using InnoSwitch™3-AQ INN3947CQ*
Specification	30 V_{DC} – 1000 V_{DC} Input; 7.5 V / 1.33 A Output
Application	Traction Inverter Gate and/or Emergency Power Supply
Author	Automotive Systems Engineering Department
Document Number	DER-946Q
Date	July 31, 2023
Revision	2.0

Summary and Features

- Ultra-compact design for 800 V_{DC} BEV automotive applications
- Low component count design (60 total components)
- Wide range input from 30 V_{DC} to 1000 V_{DC}
- Reinforced 1000 V isolated transformer (IEC-60664-1 and IEC-60664-4 compliant)
- ≥80 % efficiency across input voltage range
- Secondary-side regulated output
- Ambient operating temperature from -40 °C to 105 °C
- Fully fault protected including output current limit and short-circuit protection

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Disclaimer:

1 Introduction

This engineering report describes a 10 W single output automotive emergency power supply. It is intended for use in 800 V battery system electric vehicles supporting an ultra-wide input range of 30 V_{DC} to 1000 V_{DC}. This design utilizes the 1700 V rated INN3947CQ from the InnoSwitch3-AQ family of ICs in a flyback converter configuration.

The design provides reinforced isolation between the primary (high-voltage input) and secondary (output) sides by observing the creepage and clearance requirements as indicated in IEC-60664 parts 1 and 4.

The report contains the power supply specification, schematic diagram, printed circuit board layout, bill of materials, magnetics specifications, and performance data.

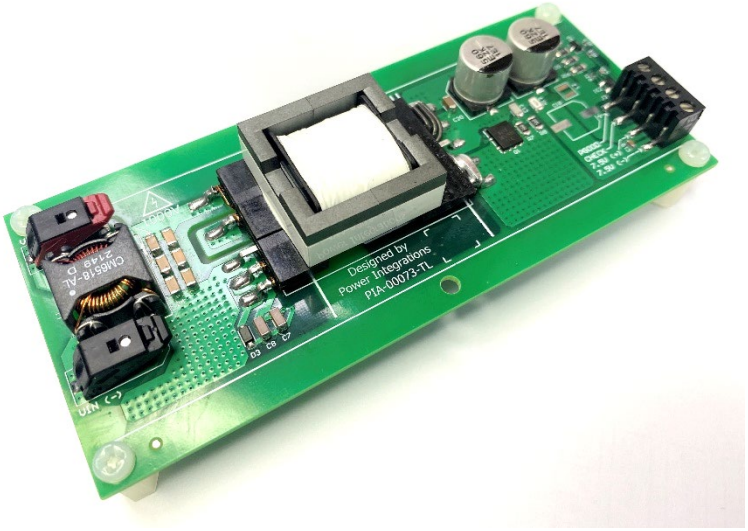


Figure 1 – Populated Circuit Board Photograph, Entire Assembly.

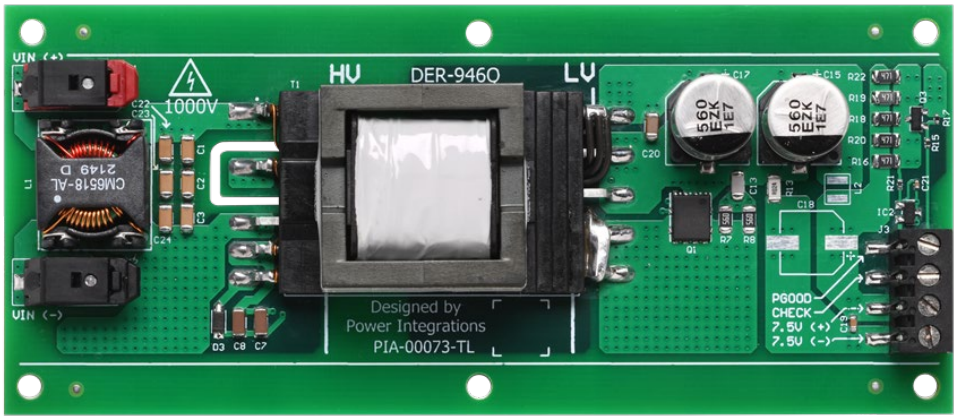


Figure 2 – Populated Circuit Board Photograph - Top.

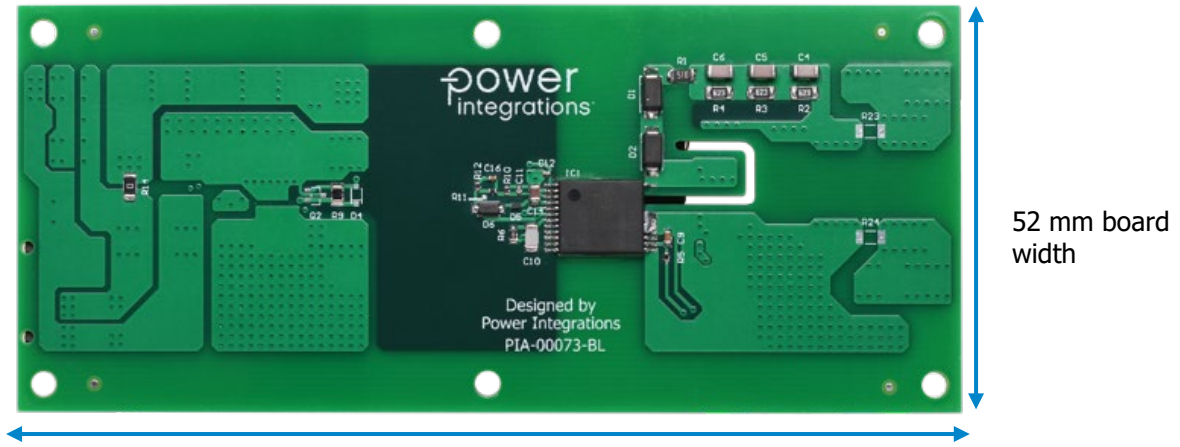


Figure 3 – Populated Circuit Board Photograph - Bottom.

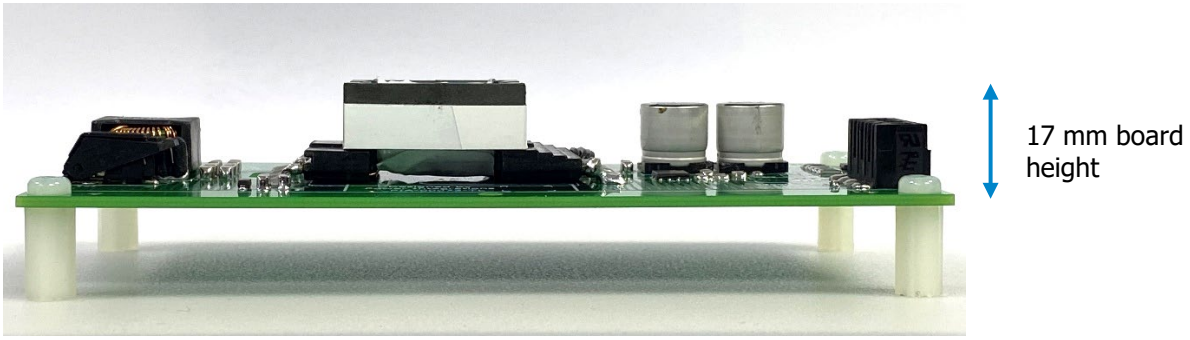


Figure 4 – Populated Circuit Board Photograph - Side.

The design can deliver the full 10 W output power up to 105 °C ambient temperature over the entire 30 V_{DC} to 1000 V_{DC} input voltage range. The 7.5 V output is typically configured to provide a redundant supply should the vehicle 12 V system supplying the traction inverter fail. This is a common requirement to meet functional safety by allowing the inverter to provide active short-circuit, active discharge and reporting functions.

The InnoSwitch3-AQ IC maintains necessary regulation by directly sensing the output voltage and providing fast, accurate feedback to the primary-side via FluxLink™. Secondary-side control also enables the use of synchronous rectification improving the overall efficiency compared to diode rectification thus saving cost and space by eliminating heat sinking.

2 Design Specification

The following tables below represent the minimum acceptable performance of the design. Actual performance is listed in the results section.

2.1 *Electrical Specifications*

Description	Symbol	Min.	Typ.	Max.	Units
Input Parameters					
Positive DC Link Input Voltage Referenced to HV - Switching Operation Conditions	**HV**	30	800	1000	V_{DC}
Operating Switching Frequency	**f_{SW}**	25		56	kHz
Output Parameters					
Output Voltage Parameters					
Regulated Output Voltage	**V_{CC}**	7.13	7.5	7.88	V_{DC}
Output Voltage Load and Line Regulation	**V_{REG}**	-5		+5	%
Ripple Voltage Measured on Board	**V_{RIPPLE}**		500		mV
Output Current Parameters					
Output Current	**I_{OUT}**		1333		mA
Output Power Parameters					
Continuous Output Power at 30 V_{DC} – 1000 V_{DC} Input	**P_{OUT}**			10	W
Output Overshoot and Undershoot During Dynamic Load Condition	**Δ V_{OUT}**		5		%

Table 1 – Electrical Specifications.

2.2 *Isolation Coordination*

Description	Symbol	Min.	Typ.	Max.	Units
Maximum Blocking Voltage of INN3947CQ	$\mathbf{BV_{DSS}}$			1700	V
System Voltage	$\mathbf{V_{SYSTEM}}$			1202	V
Working Voltage	$\mathbf{V_{WORKING}}$			1000	V
Pollution Degree	**PD**			2	
CTI for FR4	**CTI**	175		399	
Rated Impulse Voltage	$\mathbf{V_{IMPULSE}}$			2.5	kV
Altitude Correction Factor for h_a	$\mathbf{C_{ha}}$			1.59	
Technical Cleanliness Requirement				0.6	mm
Basic Clearance Distance Requirement	$\mathbf{CLR_{BASIC}}$	3.0			mm
Reinforced Clearance Distance Requirement	$\mathbf{CLR_{REINFORCED}}$	5.4			mm
Basic Creepage Distance Requirement for PCB	$\mathbf{CPG_{BASIC(PCB)}}$	5.6			mm
Reinforced Creepage Distance Requirement for PCB	$\mathbf{CPG_{REINFORCED(PCB)}}$	10.6			mm
Isolation Test Voltage Between Primary and Secondary-Side for 60s	$\mathbf{V_{ISO}}$	5000			V_{PK}
Partial Discharge Test Voltage	$\mathbf{V_{PD\_TEST}}$	1803			V_{PK}

Table 2 – Isolation Coordination[1].

2.3 *Environmental Specifications*

Description	Symbol	Min.	Typ.	Max.	Units
Ambient Temperature	Ta	-40		105	°C
Altitude of Operation	ha			5500	m
Relative Humidity	Rh			85	%

Table 3 – Environmental Specifications.

[1] Clearance and creepage distances are derived from IEC 60664-1 and IEC 60664-4.

3 Schematic

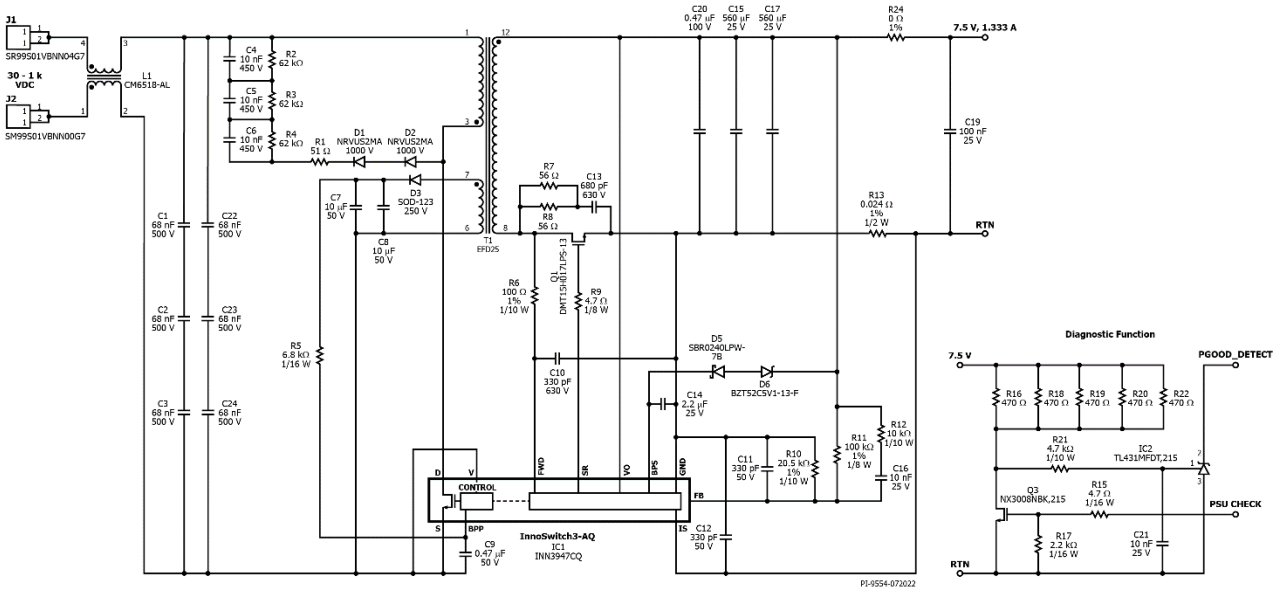


Figure 5 – DER-946Q Schematic Diagram.

4 Circuit Description

4.1 *Input Filter*

The automotive inverter environment is harsh, characterized by high dv/dt and di/dt from the switching action of the power modules. Large common mode currents are generated across the isolation barrier of the power supply which in turn can interfere with both the power supply operation, other inverter blocks and measurement signal integrity. The input common mode choke L1 together with the bypass capacitors C1 to C3 and C22 to C24 helps filter unwanted noise and prevents them from affecting the overall performance of the design.

Common mode inductor L1 was selected such that the reference board would be able to withstand the Power Integrations' internal "Resistance to ripple on high voltage network" test. The test injects high frequency ripple on the high-voltage input to simulate the actual DC link capacitor ripple in a traction inverter. The final value of L1 will depend on the final design or application requirement. The higher the noise, the higher the inductance of L1 should be. However, consideration should be given between inductance value and the DC resistance (DCR) which has an impact on the overall efficiency of the design.

Capacitor C1 to C3 and C22 to C24 bypass capacitors were selected so as not to exceed 65% of their voltage rating as well as to maintain enough pad-to-pad distance to meet creepage and clearance requirements.

4.2 *High-Voltage Side Circuit*

The design uses a flyback converter to provide an isolated low-voltage output from the high-voltage input. One end of the flyback transformer T1 primary winding is connected to the high-voltage DC input while the other end is connected to the drain terminal of the integrated 1700 V power MOSFET inside the INN3947CQ IC1.

Primary clamp circuit formed by diodes D1, D2, resistors R2, R3, and R4 and capacitors C4, C5, C6 limits the peak drain-source voltage of IC1 at the instant the switch inside IC1 turns off. As compared with the traditional RCD clamp, two surface mount AEC-Q qualified diodes were used in series to meet the creepage and clearance requirements as well as to ensure that the voltage across each diode would not exceed 70% of their rating. The resistor network helps to dissipate the energy stored in the leakage reactance of transformer T1. Snubber resistors were selected such that 80% of their voltage rating would not be exceeded while maintaining power dissipation of below 50%. Cooling areas for the snubber resistors were also considered to ensure operating temperature would be at an acceptable level.

The IC is self-starting, using an internal high-voltage current source to charge the BPP pin capacitor C9 when the DC input voltage is first applied. INN3947CQ is guaranteed to start-up from 30 V but typically will start below this level.

During normal operation, the primary-side block is powered by the auxiliary winding of transformer T1. The output of the auxiliary winding is rectified using diode D3 and filtered using capacitors C7 and C8. Resistor R5 limits the BPP pin current of IC1 to a value enough for normal operation without incurring excessive losses.

In this design the input primary under and overvoltage features were disabled by connecting the V pin to source. This approach does not require the voltage sensing resistor chain used in setting the under or overvoltage feature of IC1 thus saving cost and space. However, with no undervoltage feature the output may fail to reach regulation at voltages < 40 V_{DC} with high output load current, causing the output to rise but fail to reach regulation (hiccup). The timing is determined by the auto-restart feature, giving a 50 ms start-up attempt followed by a 2 s off time.

If this is not acceptable on the target design or application, then the undervoltage feature can be implemented. Please refer to the data sheet for the recommended circuit and design guide.

4.3 *Low-Voltage Side Circuit*

The secondary side of the INN3947CQ provides output voltage, output current sensing and gate drive for the MOSFET providing synchronous rectification (SR). The voltage across the secondary winding of the transformer T1 is rectified by the synchronous rectifier MOSFET Q1 and filtered by polymer capacitors C15 and C17. High frequency ringing during switching is reduced by the RC snubber formed by resistors R7, R8 and capacitor C13.

Switching of Q1 is controlled by the secondary-side controller inside IC1. Control is based on the winding voltage sensed by the FWD pin via resistor R6. Capacitor C10 reduces voltage spike on the FWD pin to ensure that voltage seen by this pin won't exceed its maximum rating of 150 V.

In continuous conduction mode operation, the primary-side power MOSFET is turned off just prior to the secondary-side controller commanding a new switching cycle from the primary. In discontinuous mode the SR MOSFET is turned off when the voltage drop across it falls below a certain threshold of approximately $V_{SR(TH)}$. Secondary-side control of the primary-side power MOSFET avoids any possibility of cross conduction of the two switches and ensures reliable synchronous rectifier operation.

The secondary side of the IC is self-powered from either the secondary winding forward voltage (thru R6 and the FWD pin) or by the output voltage (thru the VOUT pin). In both cases, energy is used to charge the decoupling capacitor C14 via an internal regulator.

Resistors R10 and R11 form a voltage divider network that senses the output voltage. The INN3947CQ IC has an FB pin internal reference of 1.265 V. Capacitor C11 provides decoupling from high frequency noise affecting power supply operation. C16 and R12 form

a feedforward network to speed up the feedback response time and lower the output ripple.

Output current is sensed by monitoring the voltage drop across resistor R13. The resulting current measurement is filtered with the decoupling capacitor C12 and monitored across the IS and SECONDARY GROUND pins. An internal current sense threshold of around 35 mV is used to reduce losses. Once the threshold is exceeded, the INN3947CQ IC1 will enter auto-restart (AR) operation until the load current is reduced below threshold.

4.4 *Diagnostic Circuit*

As the design will be mainly used as an emergency power supply, the design is mainly kept unloaded but must be ready to be used anytime. A diagnostic circuit is provided as a way for the system to perform self-test to check if the emergency power supply is functional or not.

An additional interface for the diagnostic circuit was added, namely: PGOOD_DETECT and PSU_CHECK. PSU_CHECK is an input signal from the system's microcontroller (3.3 V to 5 V, maximum of 8 V) used to query if the unit is functional. It drives MOSFET Q3 through resistors R15 and R17. When PSU_CHECK is HIGH, Q3 conducts and the REF pin of IC2, a TL431, is pulled low. A maximum of 0.5 W is loaded to the output via the parallel resistors R16, R18, R19, R20, and R22. Conversely, when PSU_CHECK is LOW the REF pin of IC2 is fed with the 7.5 V output voltage. R21 limits the current and C21 filters the signal to IC2's REF pin.

PGOOD_DETECT is an open collector output which must be pulled up externally (maximum of 36 V). When the REF pin of IC2 is set to HIGH (7.5 V from the main output), PGOOD_DETECT is pulled low to approximately 2 V. A pull up resistor should be selected to provide at least 1 mA. When the REF pin of IC2 is set LOW, IC2 does not conduct and PGOOD_DETECT is set to V_{CC} (pull up voltage provided). In summary, a PGOOD_DETECT LOW signal indicates that the unit is functional and ready to use while a HIGH signal indicates that the unit is not serviceable.

5 PCB Layout

Layers: Six (6) (typical for traction inverter control board)
Board Material: FR4
Board Thickness: 1.6 mm
Copper Weight: 2 oz

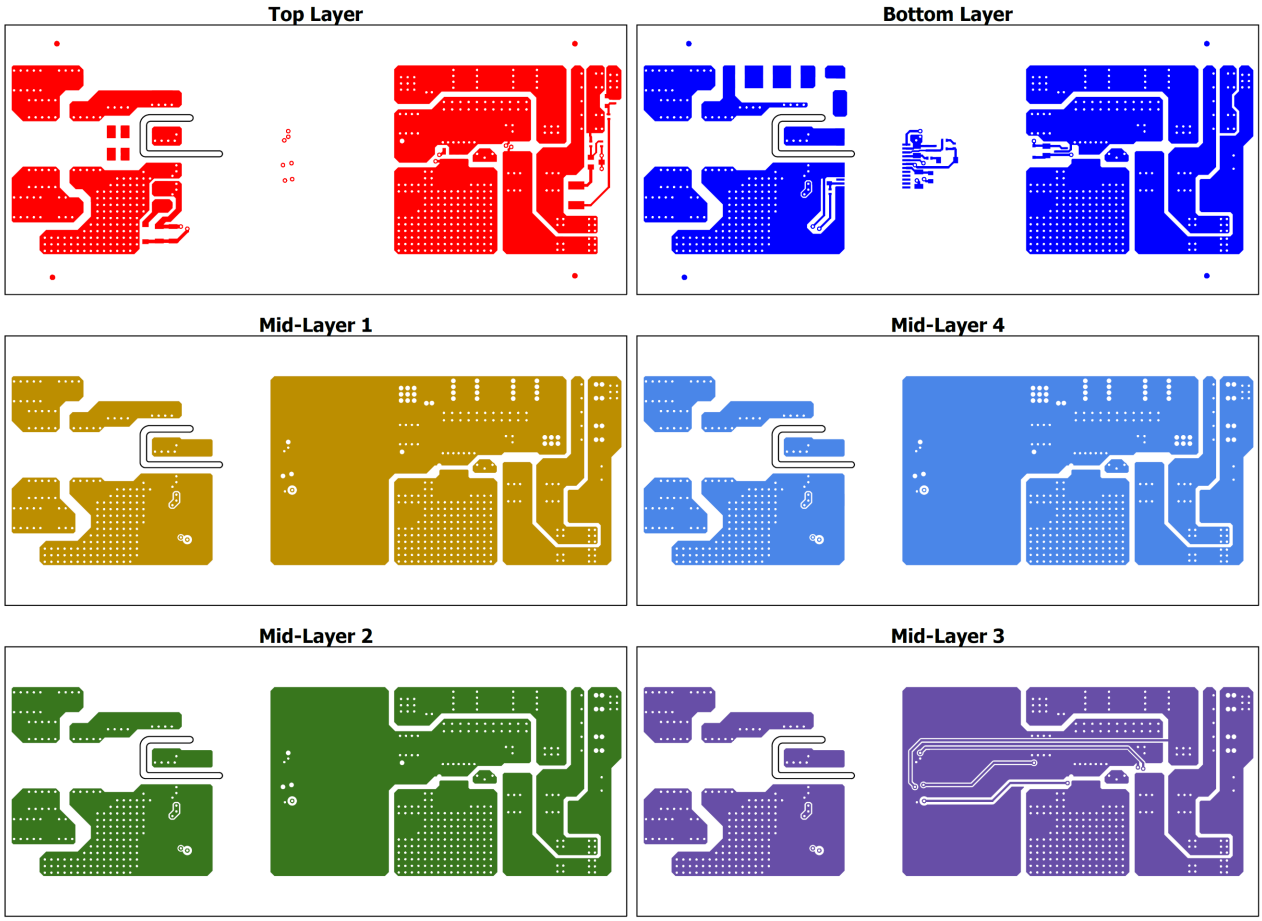


Figure 6 – DER-946Q PCB Layout.

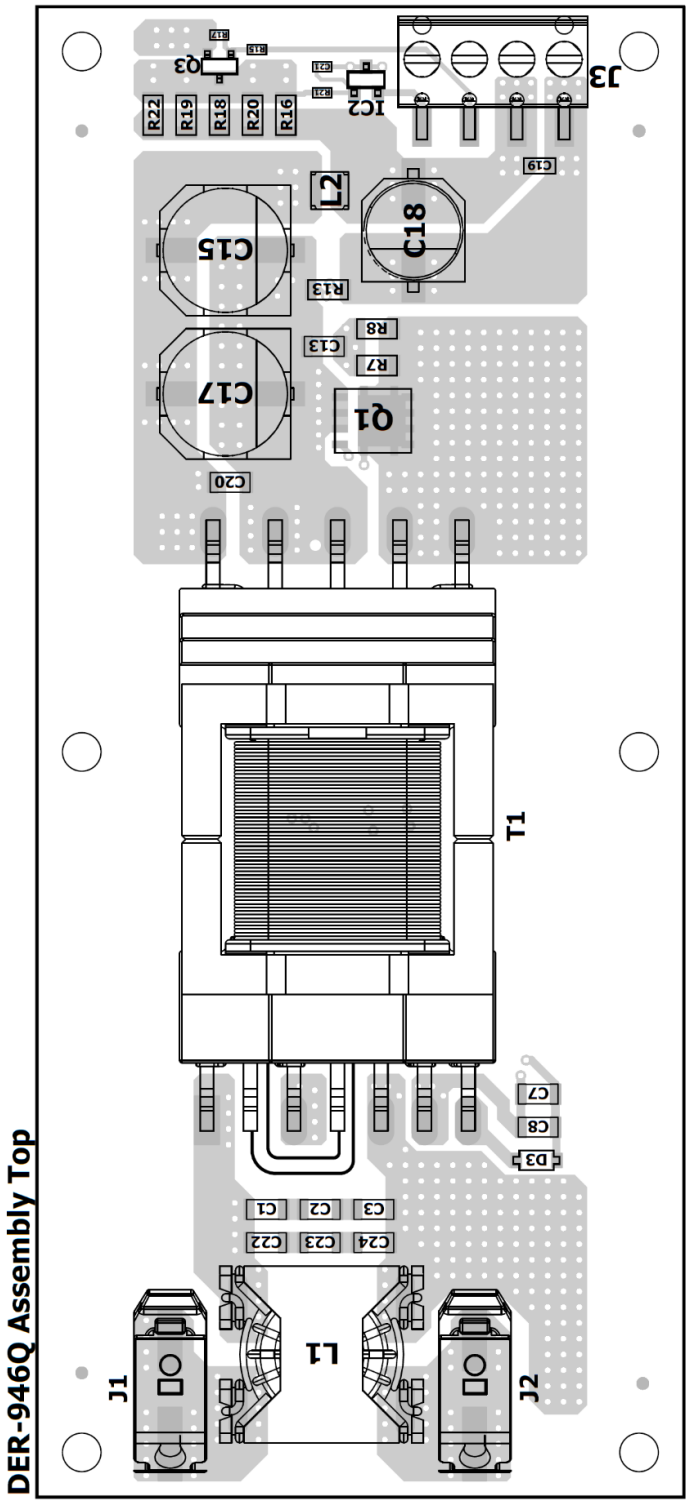


Figure 7 – DER-946Q PCB Assembly (Top).

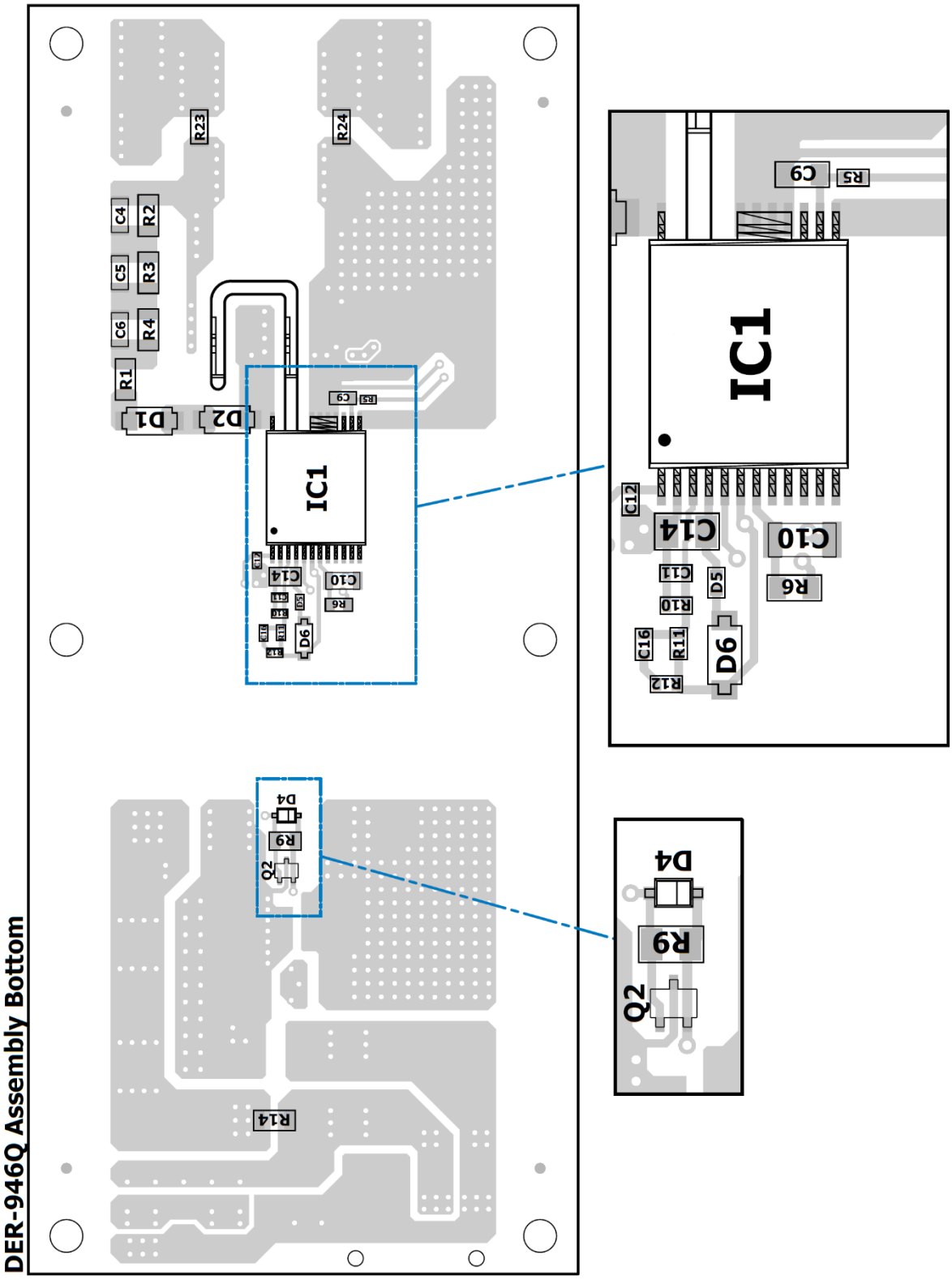


Figure 8 – DER-946Q PCB Assembly (Bottom).

6 Bill of Materials

Item	Qty	Designator	Description	MFR Part Number	Manufacturer
1	6	C1, C2, C3, C22, C23, C24	Multilayer Ceramic Capacitors MLCC - SMD/SMT 500 V 0.068 µF X7R 1206 10% AEC-Q200	C1206C683KCRACAUTO	KEMET
2	3	C4, C5, C6	Multilayer Ceramic Capacitors MLCC - SMD/SMT CGA 1206 450 V 0.01 µF C0G 5% AEC-Q200	CGA5L4C0G2W103J160AA	TDK
3	2	C7, C8	Multilayer Ceramic Capacitors MLCC - SMD/SMT 1206 50 VDC 10 µF 10% X7R AEC-Q200	CGA5L1X7R1H106K160AE	TDK
4	1	C9	Multilayer Ceramic Capacitors MLCC - SMD/SMT CGA 0603 25 V 0.47 µF X7R 10% AEC-Q200	CGA3E3X7R1E474K080AB	TDK
5	1	C10	Multilayer Ceramic Capacitors MLCC - SMD/SMT CGA 1206 630 V 330 pF C0G 5% AEC-Q200	CGA5C4C0G2J331J060AA	TDK
6	2	C11, C12	Multilayer Ceramic Capacitors MLCC - SMD/SMT 50 V 330 pF C0G 0402 5% AEC-Q200	AC0402JRNPO9BN331	YAGEO
7	1	C13	Multilayer Ceramic Capacitors MLCC - SMD/SMT 1206 630 V 680 pF 5% C0G AEC-Q200	CGA5F4C0G2J681J085AA	TDK
8	1	C14	Multilayer Ceramic Capacitors MLCC - SMD/SMT 0805 25 V 2.2 µF 10% X7R AEC-Q200	TMK212B7225KGHT	Taiyo Yuden
9	2	C15, C17	Polymer Aluminum Capacitors – 25 V 560 µF 20% AEC-Q200	B40921A5567M000	TDK
10	2	C16, C21	Multilayer Ceramic Capacitors MLCC - SMD/SMT 0402 25 V 0.01 µF 10% X7R AEC-Q200	CGA2B2X7R1E103K050BA	TDK
11	1	C19	Multilayer Ceramic Capacitors MLCC - SMD/SMT 0603 25 V 0.1 µF 10% X7R AEC-Q200	CGA3E2X7R1E104K080AA	TDK
12	1	C20	Rectifiers 1000 V 1.5 A High Efficiency Rectifier	HMK316B7474KLHT	Taiyo Yuden
13	2	D1, D2	Diode Standard 200 V 225 mA (DC) SMT SOD-123	NRVUS2MA	On Semi
14	1	D3	Diode Schottky 20 V 350 mA (DC) SMT SOD-323	BAS21GWX	Nexperia
15	1	D5	Schottky Diodes & Rectifiers 5 µA 20 V 15 A IFSM	SBR0240LPW-7B	Diodes, Inc.
16	1	D6	Schottky Diodes & Rectifiers If 1 A Vrrm 100 V	BZT52C5V1-13-F	Diodes, Inc.
17	1	IC1	CV/CC QR Flyback Switcher IC with Integrated 1700 V Switch and FluxLink Feedback for Automotive Applications	INN3947CQ	Power Integrations
18	1	IC2	Voltage References 2.495 VIN ADJ Shunt	TL431MFDT,215	Nexperia
19	1	J1	TERM BLOCK 1POS SIDE ENTRY SMD	SM99S01VBNN04G7	METZ CONNECT
20	1	J2	TERM BLOCK 1POS SIDE ENTRY SMD	SM99S01VBNN00G7	METZ CONNECT
21	1	J3	TERMI-BLOCK SMD MOUNT 180_4P_3.81	2383945-4	TE Connectivity
22	1	L1	Input Common Mode Choke	CM6518-AL	Coilcraft
23	1	Q1	N-Channel MOSFET: 150 V 9.4 A PowerDI5060-8	DMT15H017LPS-13[2]	Diodes, Inc.
24	1	Q3	N-Channel MOSFET: 30 V 400 mA SOT-23	NX3008NBK,215	Nexperia
25	1	R1	Thick Film Resistors - SMD 51 Ω ¼ W 1206 5% AEC-Q200	AC1206JR-0751RL	YAGEO
26	3	R2, R3, R4	Thick Film Resistors - SMD 1206 62 kΩ ¼ W 5% AEC-Q200	ERJ-8GEYJ623V	Panasonic
27	1	R5	Thick Film Resistors – SMD 0402 1/16 W 6.8 kΩ 5%	CRCW04027K50JNED	Vishay
28	1	R6	Thick Film Resistors - SMD 100 Ω 100 mW 0603 1% AEC-Q200	AC0603FR-13100RL	YAGEO
29	2	R7, R8	Thick Film Resistors - SMD 56 Ω ¼ W 1206 5% AEC-Q200	AC1206JR-0756RL	YAGEO
30	1	R9	Thick Film Resistors - SMD 4.7 Ω 1/8 W 0805 5% AEC-Q200	AC0805JR-074R7L	YAGEO
31	1	R10	Thick Film Resistors - SMD 20.5 kΩ 100 mW 0402 1% AEC-Q200	ERJ-2RKF2052X	Panasonic

[2] DMT15H017LPS-13 is qualified for AEC-Q101 reliability test only but not fully qualified for all AEC-Q criteria.

32	1	R11	Thick Film Resistors - SMD 0402 1% 100 kΩ AEC-Q200	SG73S1ETTP1003F	KOA
33	1	R12	Thick Film Resistors - SMD 0402 5% 10 kΩ 100 mW AEC-Q200	ERJ-U02J103X	Panasonic
34	1	R13	Current Sense Resistors – 24 mΩ 1206 ½ W 1% AEC-Q200	UCR18EVHFSR024	ROHM Semi
35	1	R14	Thick Film Resistors - SMD 0 Ω ¼ W 1206 1% AEC-Q200	AF1206JR-070RL	YAGEO
36	1	R15	Thick Film Resistors - SMD 4.7 Ω 1/16 W 0402 5% AEC-Q200	AC0402JR-074R7L	YAGEO
37	5	R16, R18, R19, R20, R22	Thick Film Resistors - SMD 470 Ω ¼ W 1206 5% AEC-Q200	CRCW1206470RJNEB	Vishay
38	1	R17	Thick Film Resistors - SMD 2.2 kΩ 1/16 W 0402 5% AEC-Q200	AC0402JR-072K2L	YAGEO
39	1	R21	Thick Film Resistors - SMD 4.7 kΩ 1/10 W 0402 5% AEC-Q200	ERJ-2GEJ472X	Panasonic
40	1	T1	10 W Power Transformer	EFD25	Power Integrations
41	2	T1-Core	3C95 Ferrite core	EFD25/13/9-3C95	Ferroxcube
42	1	T1-Bobbin	Customized bobbin	MCT-EFD25-N2 H7+5P	Power Integrations
43	1	Z1	Printed circuit board	PIA-00073-TL	Power Integrations

Table 4 – DER-946Q Bill of Materials[3].

[3] All components are AEC-Q qualified except connectors, T1 and L1.

7 Transformer Specification (T1)

7.1 *Electrical Diagram*

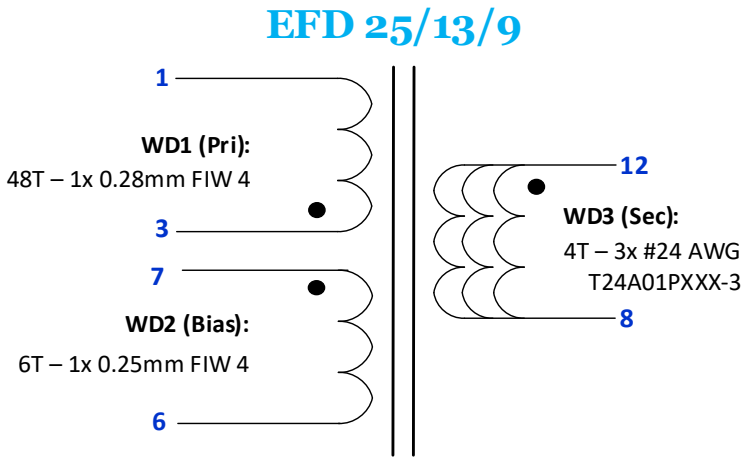


Figure 9 – Transformer Electrical Diagram.

7.2 *Electrical Specifications*

Parameter	Conditions	Min.	Typ.	Max.	Unit
Power	Output power secondary-side			10	W
Input voltage Vdc	Flyback topology	30	800	1000	V
Switching frequency	Flyback topology	25		62	kHz
Duty cycle	Flyback topology	2.3		72.6	%
Np:Ns			12		
Rdc	Primary-side		520		mΩ
Rdc	Secondary side		7.2		mΩ
Coupling capacitance	Primary-side to secondary-side Measured at 1 V_{PK-PK}, 100 kHz frequency, between pin 1 to pin 12, with pins 1 - 3 shorted and pins 8 - 12 shorted at 25 °C			25	pF
Primary inductance	Measured at 1 V_{PK-PK}, typical switching frequency, between pin 1 to pin 2, with all other windings open at 25 °C		538		µH
Part to part tolerance	Tolerance of Primary Inductance	-5.0		5.0	%
Primary leakage inductance	Measured between pin 1 to pin 3, with all other windings shorted.			8.6	µH

Table 5 – Transformer (T1) Electrical Specifications.

7.3 *Transformer Build Diagram*

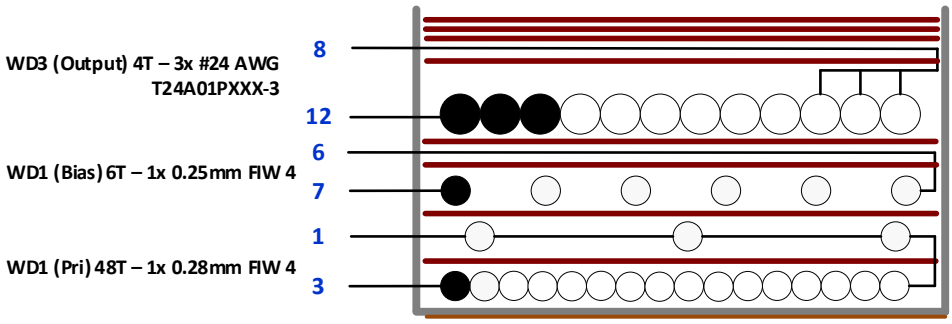


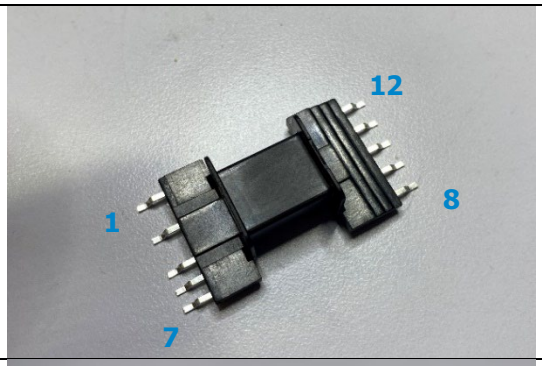
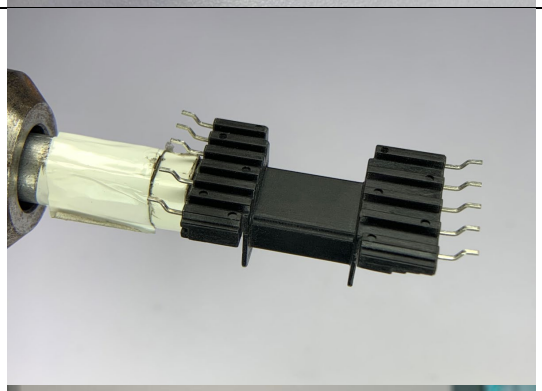
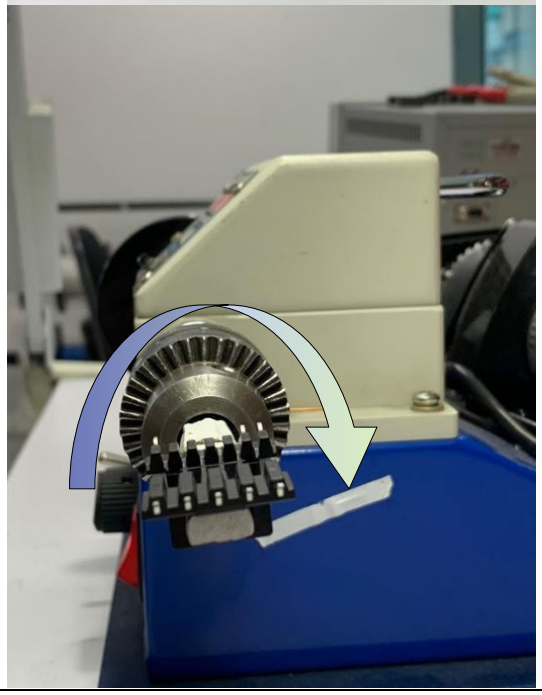
Figure 10 – Transformer Build Diagram.

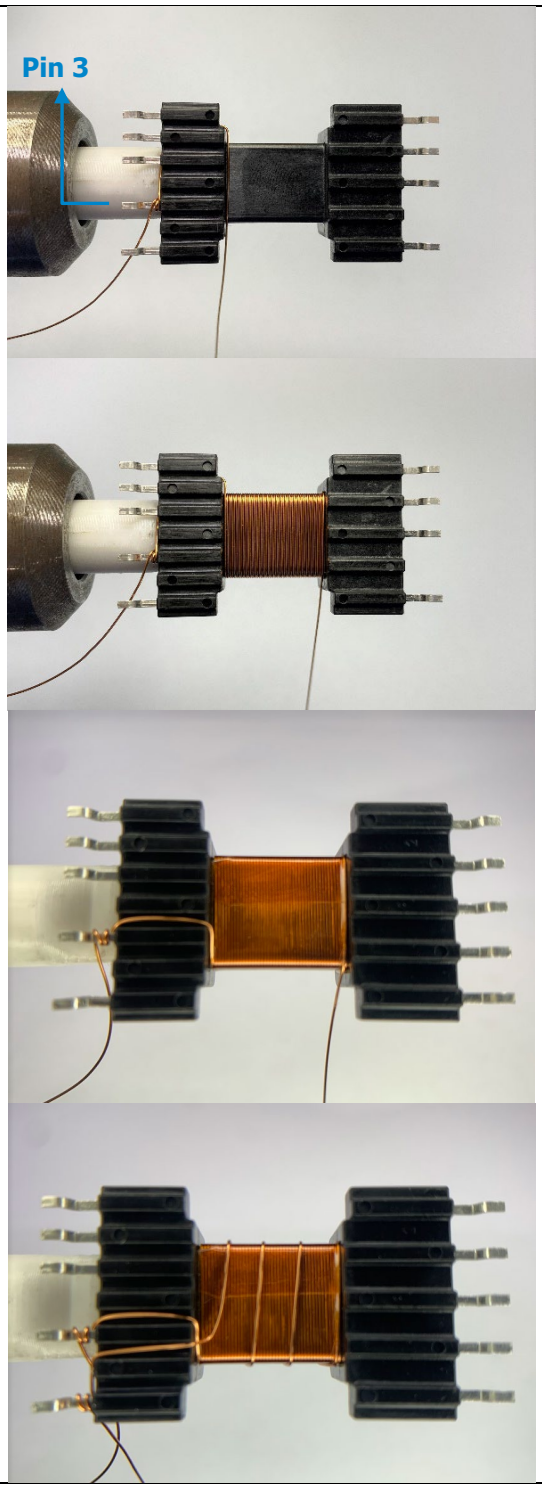
7.4 *Material List*

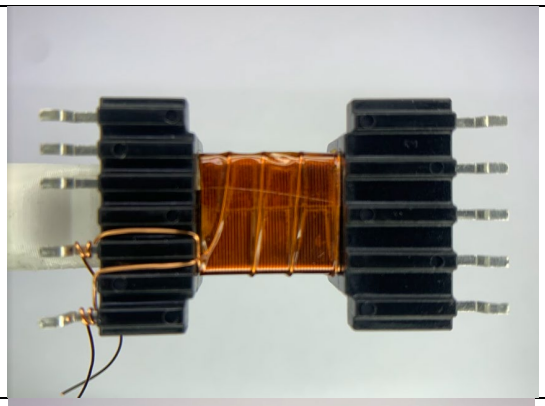
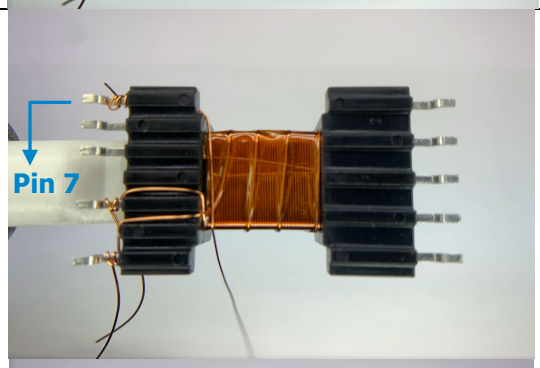
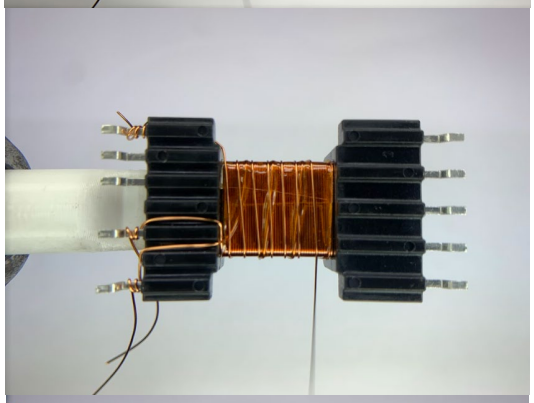
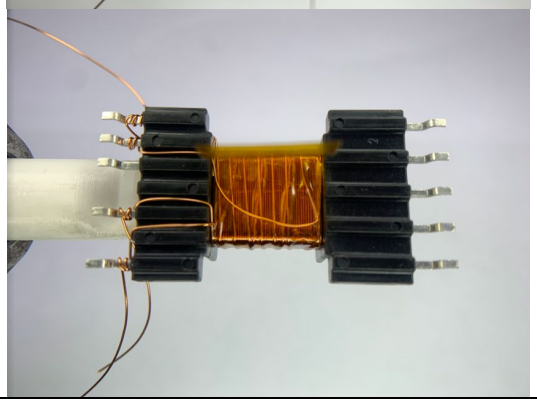
Item	Description	Qty	UOM	Material	Manufacturer
[1]	Bobbin: MCT-EFD25-N2 H7+5P	1	PC	Phenolic	MyCoilTech
[2]	Core: EFD 25/13/9	2	PCS	3C95 (or equivalent)	Ferroxcube
[3]	WD1 (Pri): 0.28 mm FIW 4, Class F	2200	mm	Copper Wire	Elektrisola
[4]	WD2 (Bias): 0.25 mm FIW 4, Class F	330	mm		Elektrisola
[5]	WD3a (Sec): T24A01PXXX-3, AWG 24 PFA.003”	900	mm		Rubadue
[6]	3M Polyimide 5413 Amber, width: 0.625in (15.9mm)	360	mm	3M157181 (or equivalent)	3M

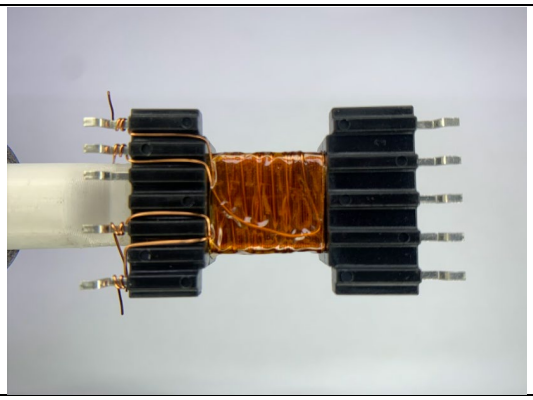
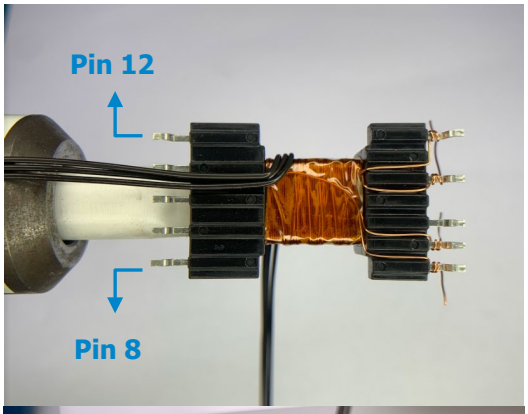
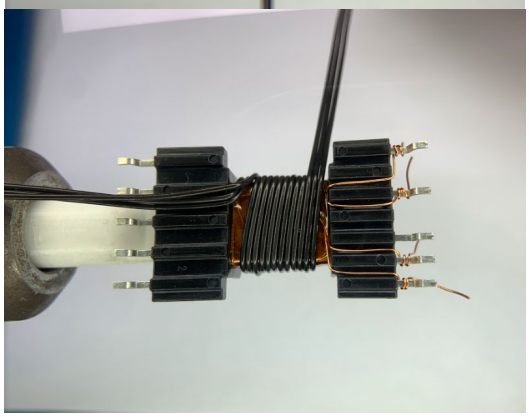
Table 6 – Transformer (T1) Material List.

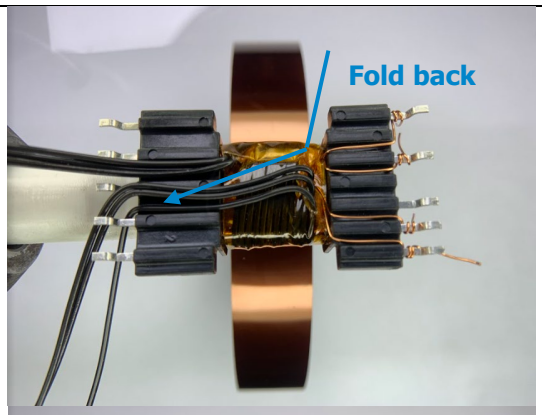
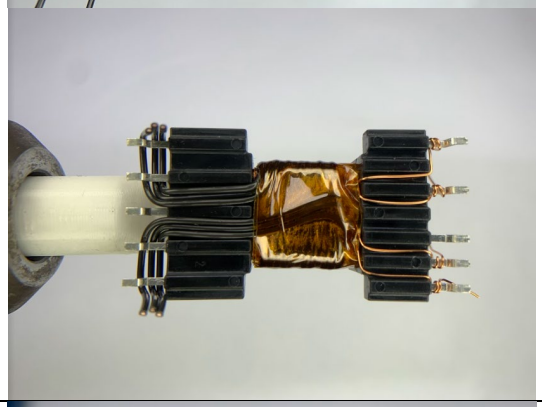
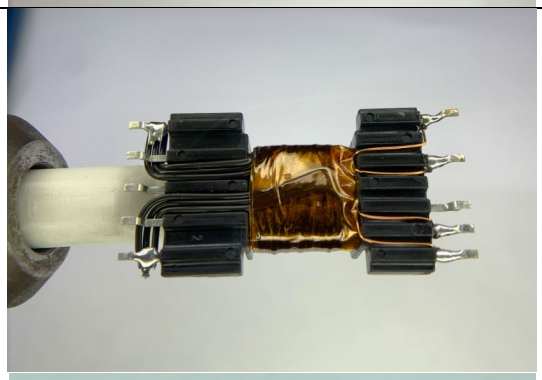
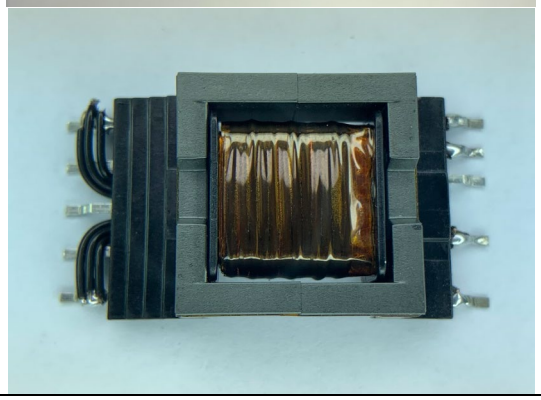
7.5 *Winding Instructions*

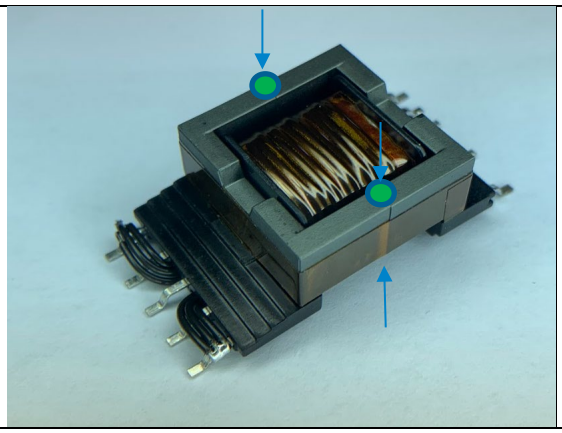
Winding Preparation		Start by removing the unused pins 2, and 4 of the bobbin (Item [1])
Winding Preparation	 	Position the bobbin on the mandrel such that the primary side (pins 1-7) of the bobbin is on the left side. Winding direction is clockwise direction.

WD1: Pri		Start at pin 3, initially route the wire on the other side of the bobbin. Use a single strand of wire Item [3] and wind 45 turns with tight tension, from left to right. This should fit the entire bobbin's width. Secure the wire and apply 1 layer of tape (Item [6]) then wind the remaining 3 turns with tight tension and spread equally across the bobbin width. Terminate at pin 1 by routing on the groove between pins 2 and 3. Reroute the other end of the wire via the groove between pins 3 and 4 then terminate again on pin 3. Place 1 layer of tape (Item [6]).

		
WD2: Bias	  	Start at pin 7, passing on the other side of the bobbin temporarily. Using a single strand of Item [4], Wind 6 turns with tight tension, from left to right. Spread the winding evenly along the bobbin's width. Partially apply 1 layer of tape (Item [6]) before terminating the winding back to pin 6. Remove the termination on pin 7 and place it on the bottom side of the bobbin before terminating it again. Finish applying 1 layer of tape (Item [6]).

		
WD3: Sec	 	Before winding, it is advised to invert the bobbin placement on the winding machine to secure the wire on the machine itself. This will make winding much easier. Also, since the bobbin is inverted, the winding direction needs to be inverted (counterclockwise). Use 3 strands of wire Item [5] for the output winding and start it at pin 12. Route the wires via the groove between pins 10 and 11. Wind 4 turns with tight tension, from left to right. Spread the winding evenly along the bobbin's width. Partially apply 1 layer of tape (Item [6]) before terminating the winding back to pin 8, routing across the groove between pins 9 and 10. Then place another 3 layers of tape (Item [6]) on top. It is advised to remove the wire's insulation before terminating on the respective pins for cleaner and easier soldering.

	 	
Finishing	 	Solder all terminated pins (pin 1, 3, 6, 7, 8, 9, and 12). Gap one of the core halves (item [2]) and fasten the core tightly to get 538 µH ± 5% of inductance between pins 1 and 3. In fastening the core, it is preferred to use glue instead of tape that is used in the illustration (see blue arrows for the preferred gluing points – 2 points on top and 2 points on the bottom.)

8 Transformer Design Spreadsheet

1	DCDC_InnoSwitch3AQ1700V_Flyback_120821; Rev.2.2; Copyright Power Integrations 2021	INPUT	INFO	OUTPUT	UNITS	InnoSwitch3-AQ1700V Flyback Design Spreadsheet
2	**APPLICATION VARIABLES**					
3	VOUT	7.50		7.50	V	Output Voltage
4	**OPERATING CONDITION 1**					
5	VINDC1	1000.00		1000.00	V	Input DC voltage 1
6	IOUT1	1.333		1.333	A	Output current 1
7	POUT1			10.00	W	Output power 1
8	EFFICIENCY1			0.85		Converter efficiency for output 1
9	Z_FACTOR1			0.50		Z-factor for output 1
11	**OPERATING CONDITION 2**					
12	VINDC2	30.00		30.00	V	Input DC voltage 2
13	IOUT2	1.333		1.333	A	Output current 2
14	POUT2			10.00	W	Output power 2
15	EFFICIENCY2			0.85		Converter efficiency for output 2
16	Z_FACTOR2			0.50		Z-factor for output 2
69	**PRIMARY CONTROLLER SELECTION**					
70	ENCLOSURE			ADAPTER		Power supply enclosure
71	ILIMIT_MODE	STANDARD		STANDARD		Device current limit mode
72	VDRAIN_BREAKDOWN			1700	V	Device breakdown voltage
73	DEVICE_CODE	INN3947CQ		INN3947CQ		Device code
74	PDEVICE_MAX			50	W	Device maximum power capability
75	RDSON_25DEG			1.53	Ω	Primary switch on-time resistance at 25°C
76	RDSON_100DEG			2.72	Ω	Primary switch on-time resistance at 100°C
77	ILIMIT_MIN			1.488	A	Primary switch minimum current limit
78	ILIMIT_TYP			1.600	A	Primary switch typical current limit
79	ILIMIT_MAX			1.712	A	Primary switch maximum current limit
80	VDRAIN_ON_PRSW			1.02	V	Primary switch on-time voltage drop
81	VDRAIN_OFF_PRSW			1130	V	Peak drain voltage on the primary switch during turn-off
85	**WORST CASE ELECTRICAL PARAMETERS**					
86	FSWITCHING_MAX	31000		31000	Hz	Maximum switching frequency at full load and the valley of the minimum input AC voltage
87	VOR	90.0		90.0	V	Voltage reflected to the primary winding (corresponding to set-point 1) when the primary switch turns off
88	KP			1.633		Measure of continuous/discontinuous mode of operation
89	MODE_OPERATION			DCM		Mode of operation
90	DUTYCYCLE			0.655		Primary switch duty cycle
91	TIME_ON_MIN			0.60	us	Minimum primary switch on-time
92	TIME_ON_MAX		Info	24.01	us	Maximum primary switch on-time is greater than 11.75 us: Increase the controller switching frequency or increase the VOR
93	TIME_OFF			11.58	us	Primary switch off-time
94	LPRIMARY_MIN			511.3	uH	Minimum primary magnetizing inductance
95	LPRIMARY_TYP			538.2	uH	Typical primary magnetizing inductance
96	LPRIMARY_TOL			5.0	%	Primary magnetizing inductance tolerance
97	LPRIMARY_MAX			565.2	uH	Maximum primary magnetizing inductance
99	**PRIMARY CURRENT**					
100	IAVG_PRIMARY			1.263	A	Primary switch average current
101	IPEAK_PRIMARY			1.263	A	Primary switch peak current
102	IPEDESTAL_PRIMARY			0.375	A	Primary switch current pedestal
103	IRIPPLE_PRIMARY			1.263	A	Primary switch ripple current
104	IRMS_PRIMARY			0.562	A	Primary switch RMS current

106	**SECONDARY CURRENT**					
107	IPEAK_SECONDARY			15.152	A	Secondary winding peak current
108	IPEDESTAL_SECONDARY			0.000	A	Secondary winding pedestal current
109	IRMS_SECONDARY			3.828	A	Secondary winding RMS current
110	IRIPPLE_CAP_OUT			3.588	A	Output capacitor ripple current
113	**TRANSFORMER CONSTRUCTION PARAMETERS**					
114	**CORE SELECTION**					
115	CORE	CUSTOM	Info	CUSTOM		The transformer windings may not fit: pick a bigger core or bobbin and refer to the Transformer Parameters tab for fit calculations
116	CORE NAME	EFD 25/13/9-3C95		EFD 25/13/9-3C95		Core code
117	AE	58.0		58.0	mm^2	Core cross sectional area
118	LE	57.0		57.0	mm	Core magnetic path length
119	AL	2660		2660	nH	Ungapped core effective inductance per turns squared
120	VE	3300		3300	mm^3	Core volume
121	BOBBIN NAME	MCT-EFD25-N2 H7+P5		MCT-EFD25-N2 H7+P5		Bobbin name
122	AW	38.5		38.5	mm^2	Bobbin window area
123	BW	16.20		16.20	mm	Bobbin width
124	MARGIN			0.0	mm	Bobbin safety margin
126	**PRIMARY WINDING**					
127	NPRIMARY			48		Primary winding number of turns
128	BPEAK			3557	Gauss	Peak flux density
129	BMAX			2500	Gauss	Maximum flux density
130	BAC			1250	Gauss	AC flux density (0.5 x Peak to Peak)
131	ALG			234	nH	Typical gapped core effective inductance per turns squared
132	LG			0.285	mm	Core gap length
133	LAYERS_PRIMARY			1		Primary winding number of layers
134	AWG_PRIMARY			29		Primary wire gauge
135	OD_PRIMARY_INSULATED			0.337	mm	Primary wire insulated outer diameter
136	OD_PRIMARY_BARE			0.286	mm	Primary wire bare outer diameter
137	CMA_PRIMARY			225.4	Cmils/A	Primary winding wire CMA
139	**SECONDARY WINDING**					
140	NSECONDARY			4		Secondary winding number of turns
141	AWG_SECONDARY			21		Secondary wire gauge
142	OD_SECONDARY_INSULATED			1.029	mm	Secondary wire insulated outer diameter
143	OD_SECONDARY_BARE			0.723	mm	Secondary wire bare outer diameter
144	CMA_SECONDARY			211.6	Cmils/A	Secondary winding wire CMA
146	**BIAS WINDING**					
147	NBIAS			6		Bias winding number of turns
151	**PRIMARY COMPONENTS SELECTION**					
152	**BIAS WINDING**					
153	VBIAS			9.00	V	Rectified bias voltage
154	VF_BIAS	1.00		1.00	V	Bias winding diode forward drop
155	VREVERSE_BIASDIODE			134.00	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
156	CBIAS			22	uF	Bias winding rectification capacitor
157	CBPP			0.47	uF	BPP pin capacitor
161	**SECONDARY COMPONENTS SELECTION**					
162	RECTIFIER					
163	VDRAIN_OFF_SRFET			109.00	V	Secondary rectifier reverse voltage (accounting for a 20% parasitic voltage ring)
164	SRFET	Auto		DMT12H007LPS-13		Secondary rectifier (Logic MOSFET)

165	VBREAKDOWN_SRFET			120	V	Secondary rectifier breakdown voltage
166	RDSON_SRFET			14.1	mΩ	SRFET on time drain resistance at 25degC for VGS=4.4V
168	**FEEDBACK COMPONENTS**					
169	RFB_UPPER			100.00	kΩ	Upper feedback resistor (connected to the output terminal)
170	RFB_LOWER			20.50	kΩ	Lower feedback resistor
171	CFB_LOWER			330	pF	Lower feedback resistor decoupling capacitor

Table 7 – DER-946Q PIXls Spreadsheet.

9 Performance Data

Note: 1. Measurements were taken with the unit under test set-up inside a thermal chamber placed inside a High Voltage (HV) room.

Figure 11 – High Voltage Test Set-up.

Figure 12 – Test Set-up Inside the High Voltage Room.

2. Unit under test was placed under a box while inside the thermal chamber to eliminate the effect of any airflow.

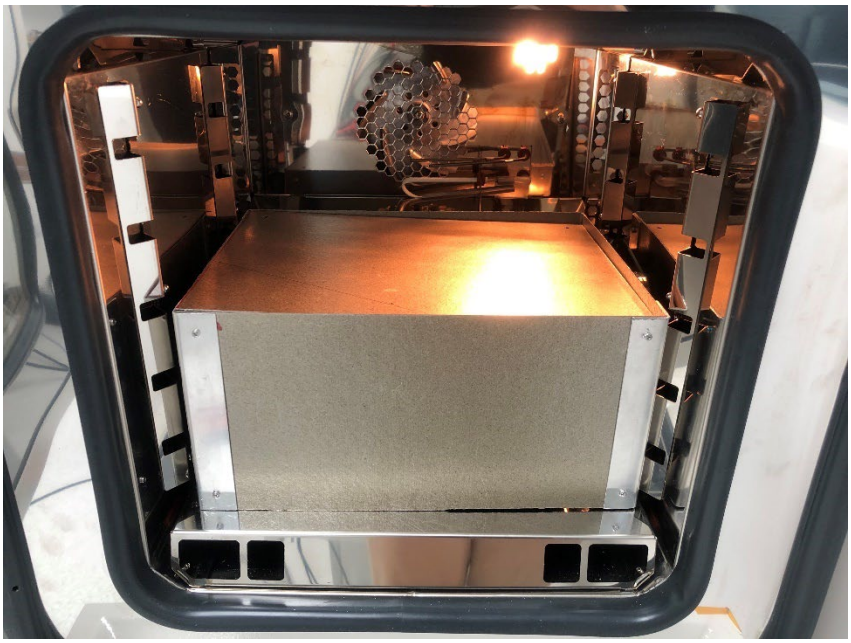


Figure 13 – Unit under test placed under a box to eliminate the effect of airflow.

3. For data points showing performance across varying input line voltages and output load currents, the unit under test was soaked at full load condition for at least 5 min. for every change in the input voltage during the start of every test sequence. Also, for every loading condition, unit under test was soaked for at least 20 s before measurements were taken.

9.1 *No-Load Input Power*

Figure 14 shows the test set up diagram for no load input current acquisition. The voltage metering point is placed before the ammeter; this is done to prevent the voltage sensing bias current from affecting the input current measurement. The ammeter used was Tektronix DMM 4050 6-1/2 Digit Precision Multimeter.

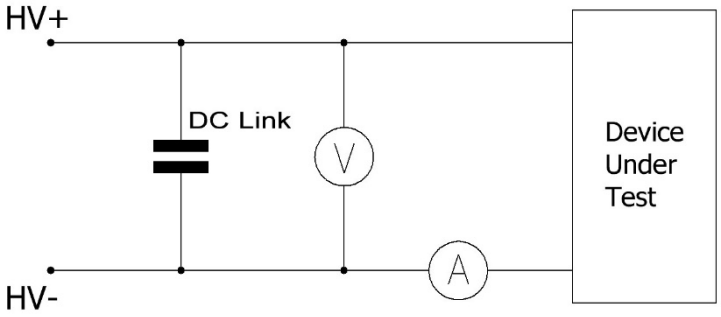


Figure 14 - No-Load Input Power Measurement Diagram.

The unit was soaked for ten minutes before starting data averaging of fifty thousand samples over a period of one minute. Analog filtering is also enabled to improve measurement accuracy.

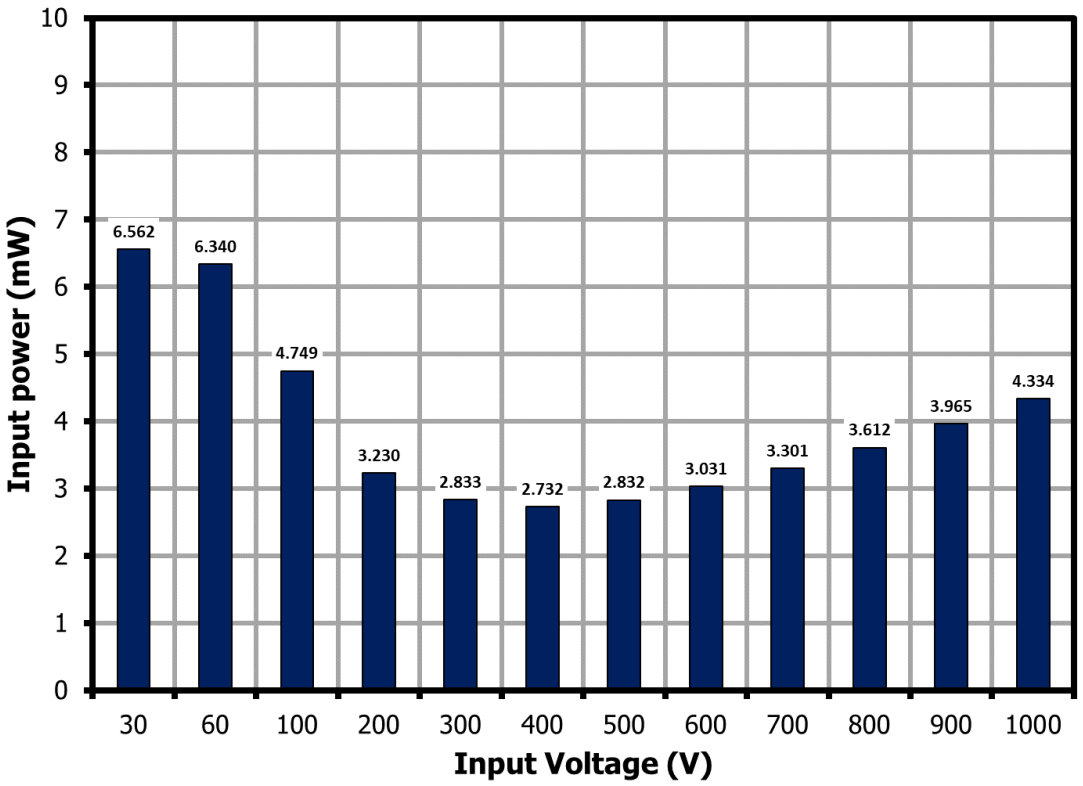


Figure 15 – No-Load Input Power vs. Input Voltage.

9.2 *Efficiency*

9.2.1 Line Efficiency

Line efficiency describes how the change in input voltage affects the overall efficiency of the unit.

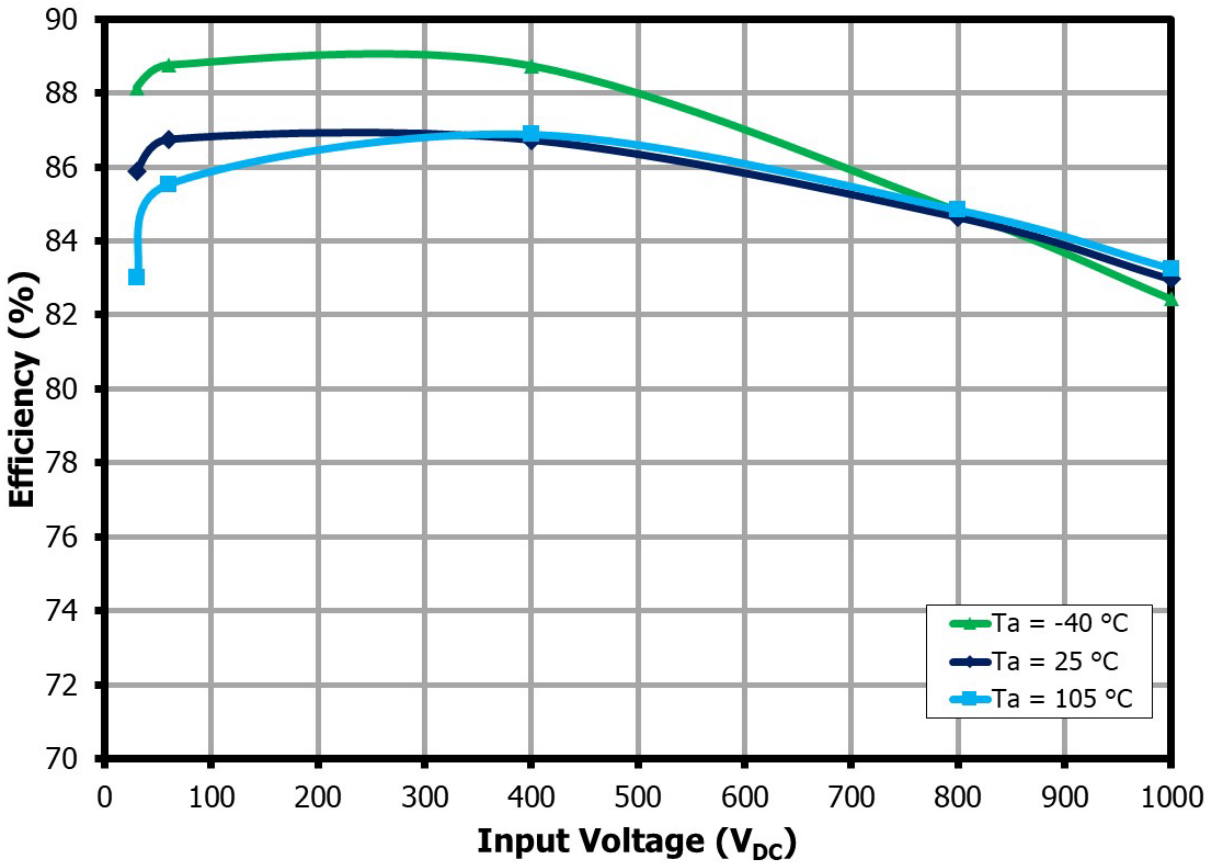


Figure 16 – Full Load Efficiency vs. Input Line Voltage.

9.2.2 Load Efficiency

Load efficiency describes how the change in output loading conditions affects the overall efficiency of the unit.

9.2.2.1 Efficiency vs. Load at 105 °C Ambient

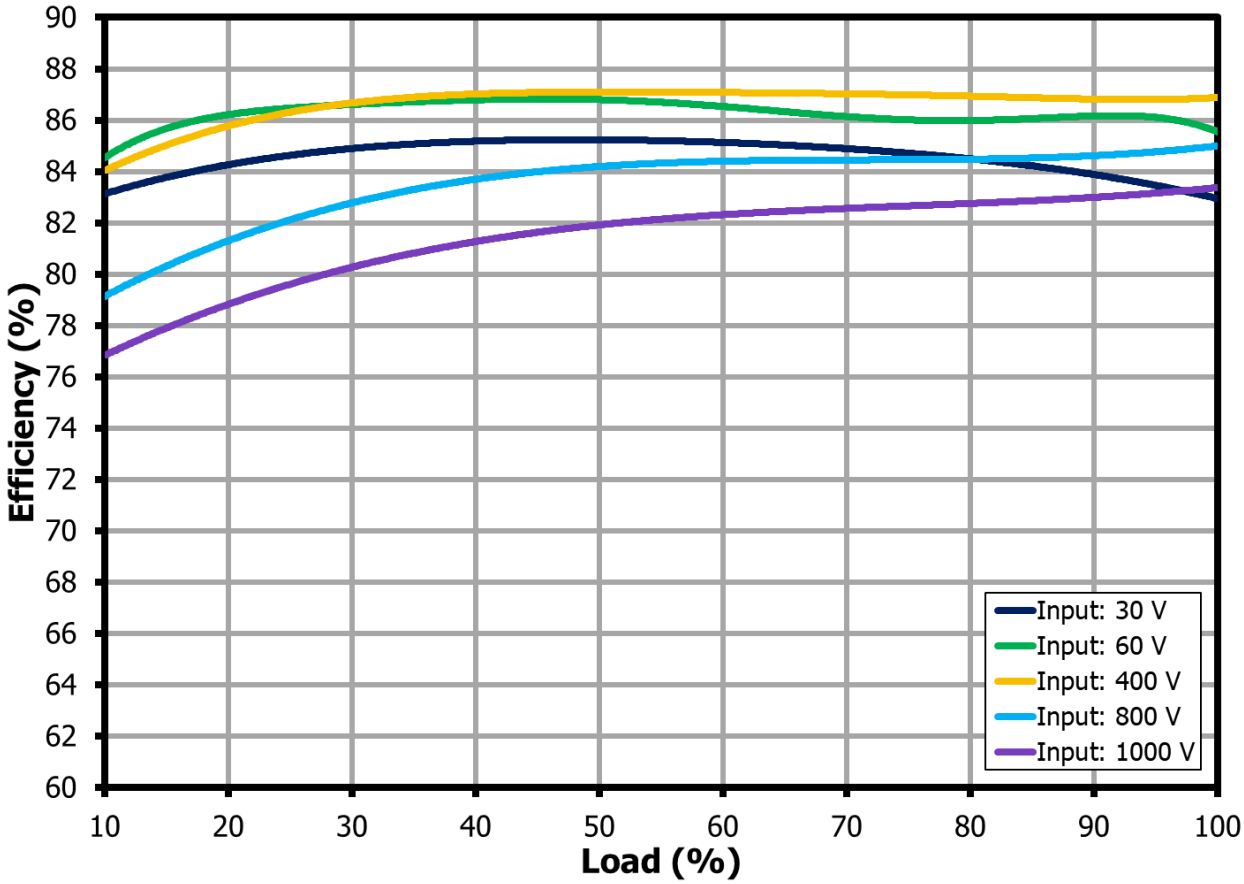


Figure 17 – Efficiency vs. Load at Different Input Voltages (105 °C Ambient).

9.2.2.2 Efficiency vs. Load at 25 °C Ambient

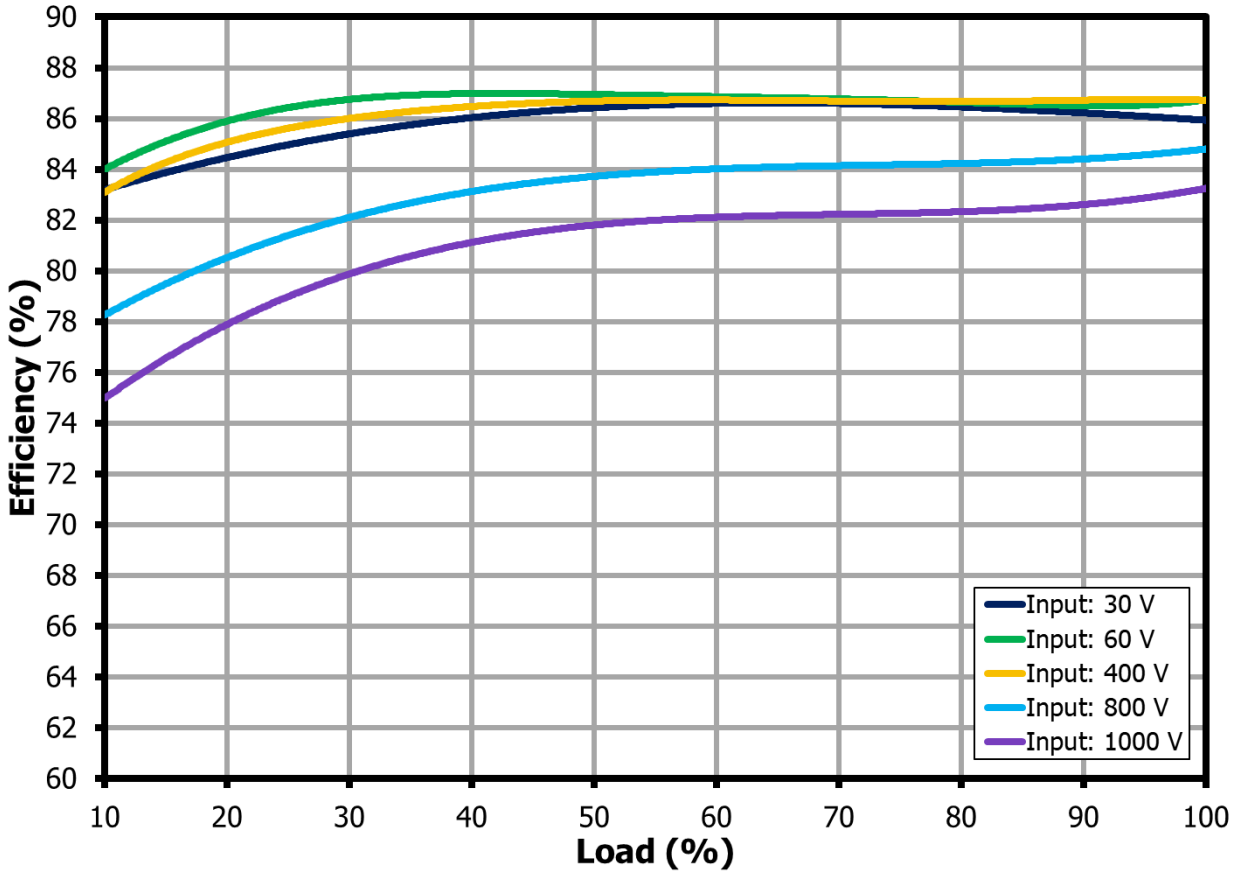


Figure 18 – Efficiency vs. Load at Different Input Voltages (25 °C Ambient).

9.2.2.3 Efficiency vs. Load at -40 °C Ambient

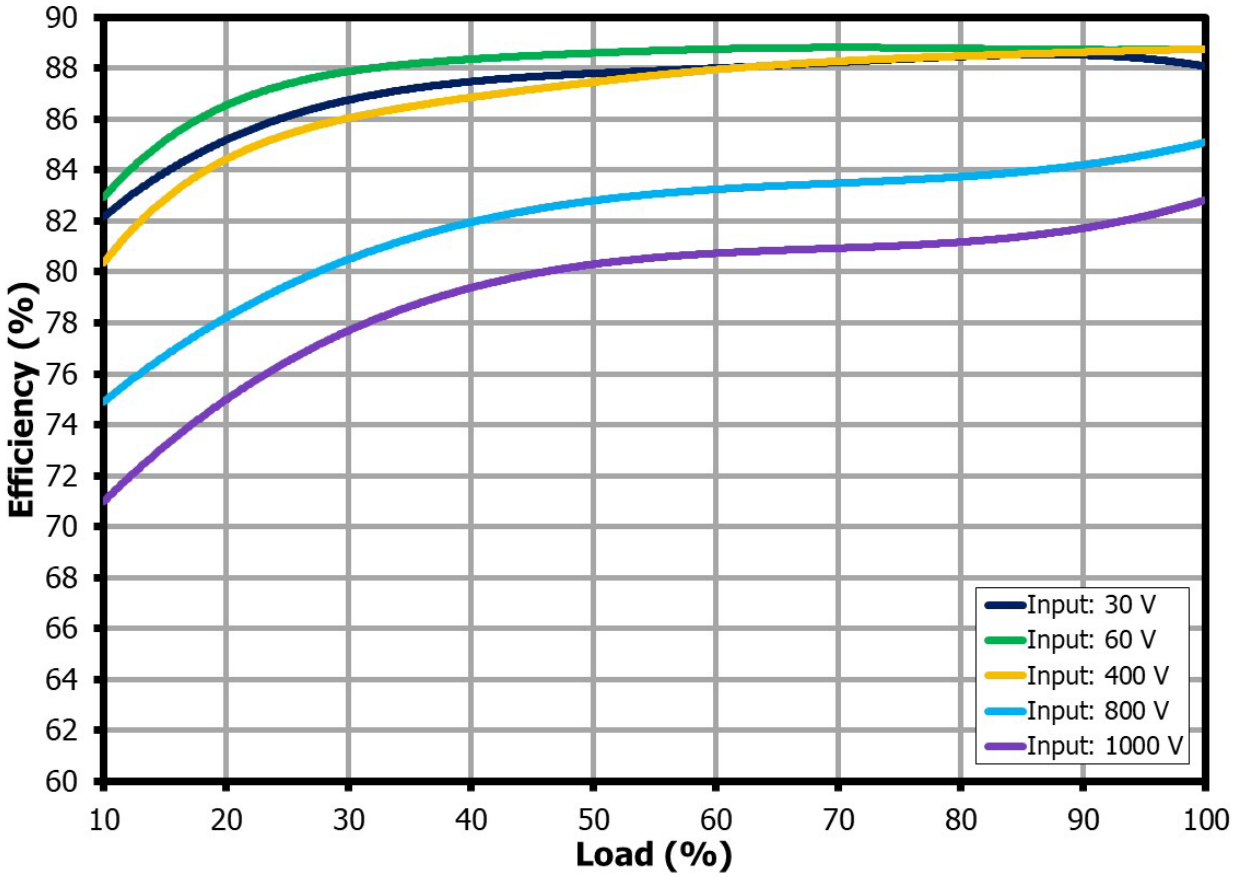


Figure 19 – Efficiency vs. Load at Different Input Voltages (-40 °C Ambient).

9.3 *Output Line and Load Regulation at 105 °C Ambient*

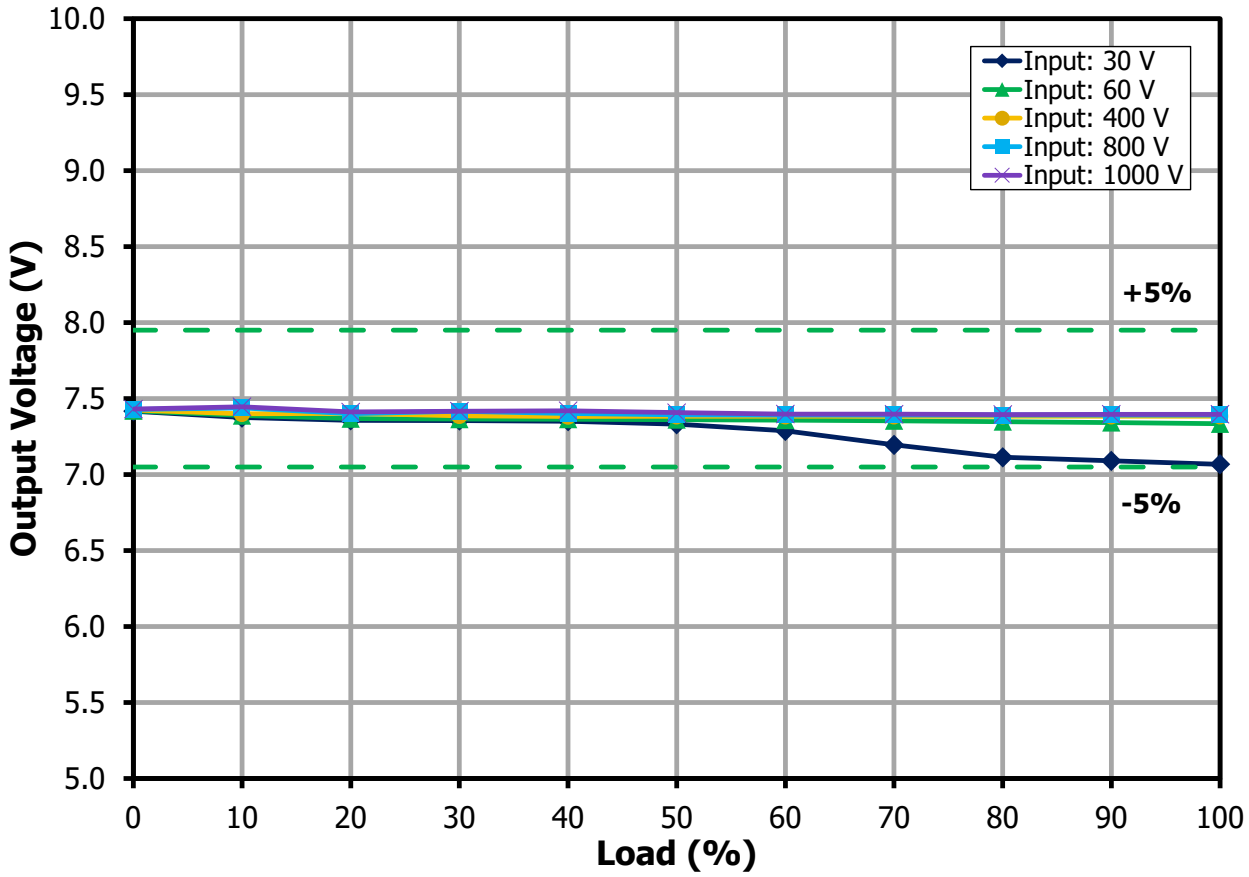


Figure 20 – Output Regulation vs. Load at Different Input Voltages (105 °C Ambient).

9.4 *Output Line and Load Regulation at 25 °C Ambient*

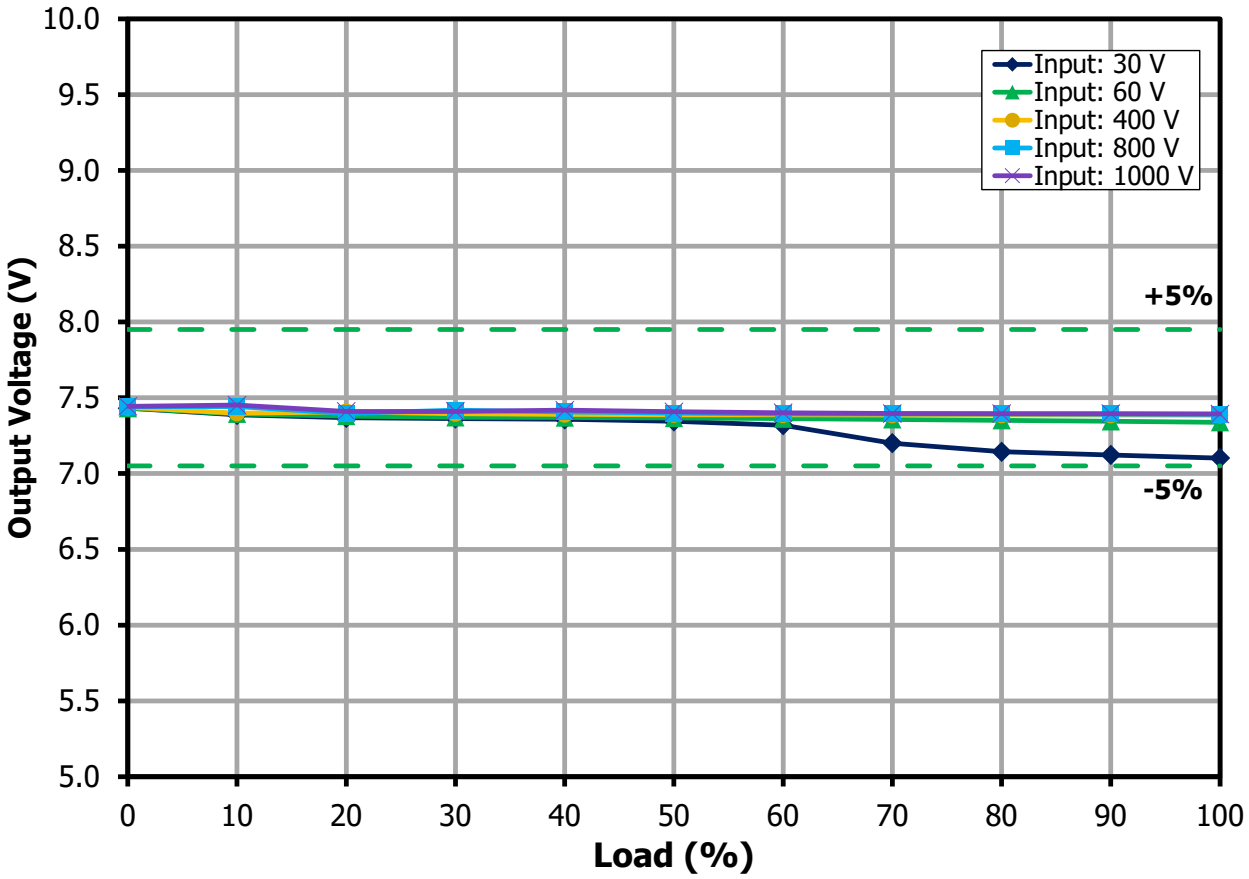


Figure 21 – Output Regulation vs. Load vs. Line Voltage (25 °C Ambient).

9.5 *Output Line and Load Regulation at -40 °C Ambient*

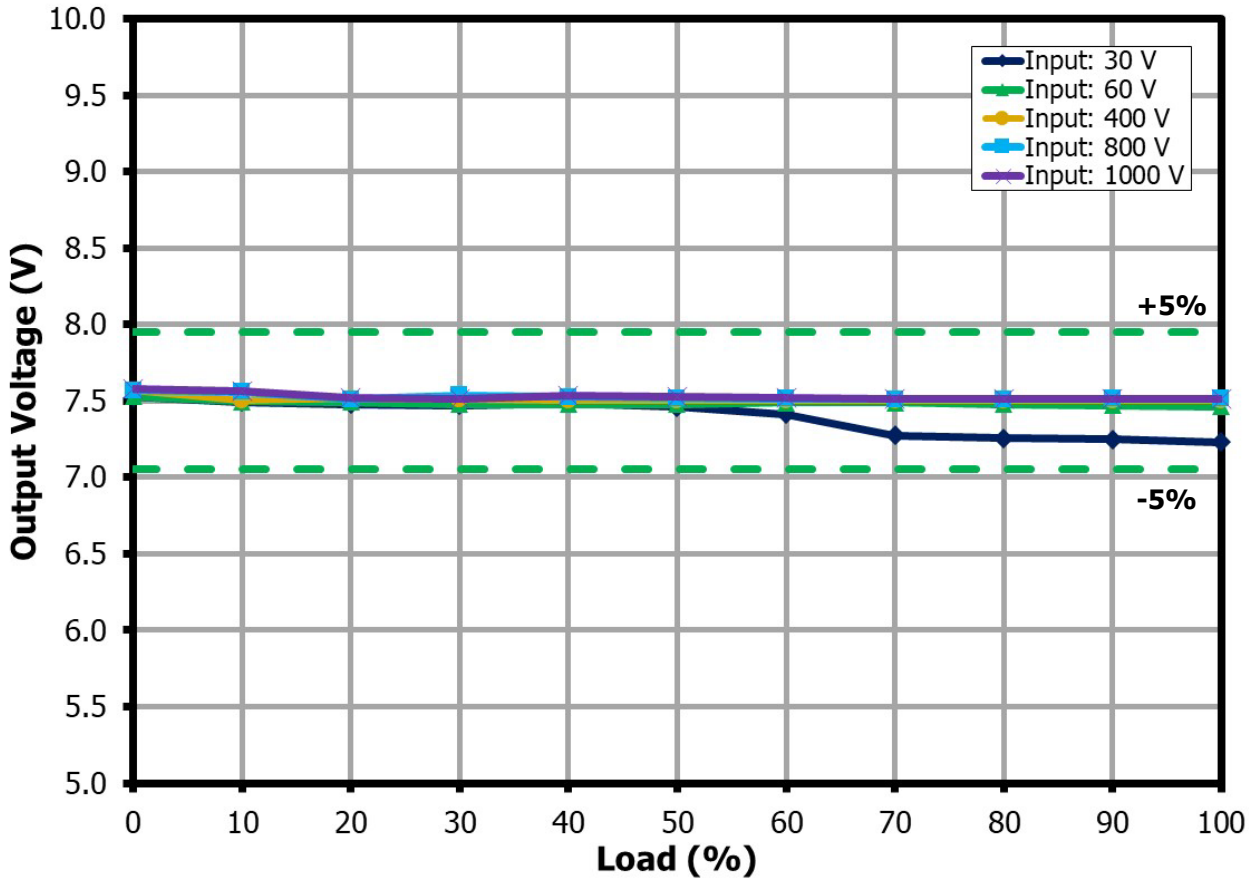


Figure 22 – Output Regulation vs. Load vs. Line Voltage (-40 °C Ambient).

10 Thermal Performance

10.1 *Thermal Data at 105 °C Ambient Temperature*

The unit was placed inside a thermal chamber and soaked for at least 1 hour to allow component temperatures to settle.

Critical components	Input Voltage		
	30 V	800 V	1000 V
Primary Snubber Resistor	117.2	120	121.45
InnoSwitch3-AQ	125.7[4]	123.55	127.35[4]
Transformer Core	114.7	122.7	124.75
Transformer Wire	117.25	123.95	126.5
SR FET	115.9	122.85	124.9
Secondary Snubber Resistor	114.15	122.5	125.15
Output Capacitor	112.35	119.9	120.95
Input CMC	114.95	121.7	122.7
Ambient Temperature	105.55	106.35	107.35

Table 8 – Thermals Data at 105 °C at Different Input Voltages.

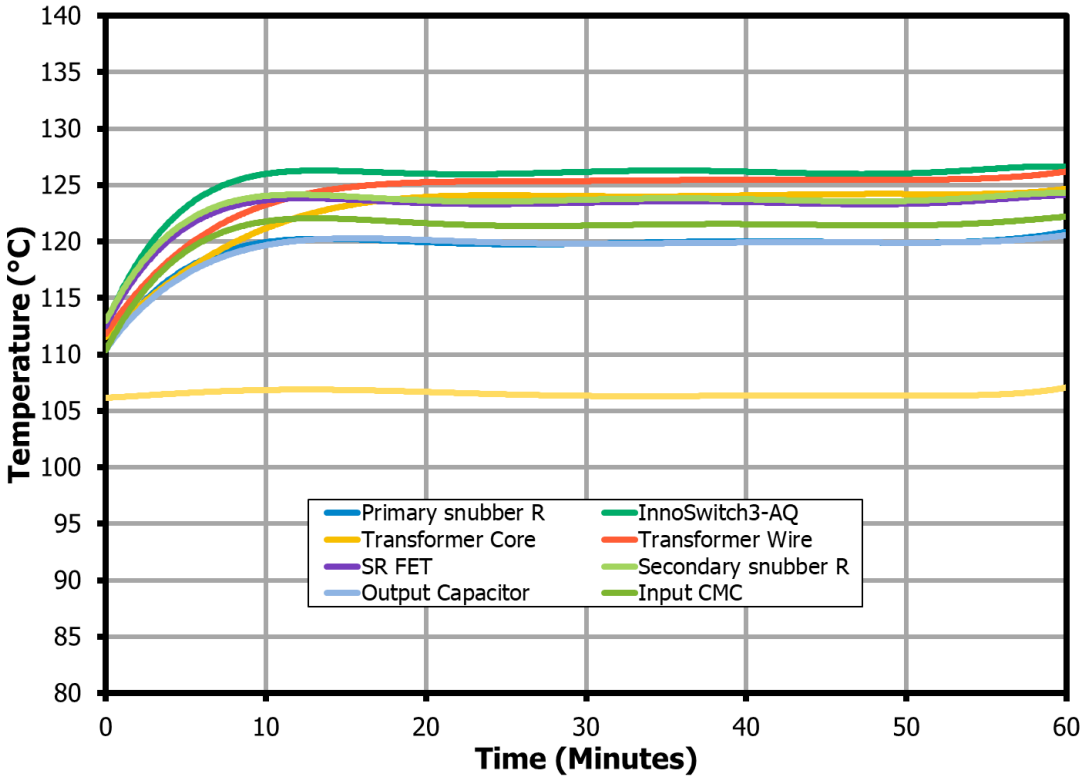


Figure 23 – Component Temperatures at 105 °C Ambient, 1000 V Input.

[4] Increasing the cooling area in the actual design or having a provision for heatsink or thermal pad between source pad and thermal area of the device and the enclosure is recommended.

10.2 *Thermals Data at 25 °C Ambient Temperature*

The following thermal scans are captured using a Fluke thermal imager after soaking for at least 1 hour in an enclosure to minimize the effect of air flow.

Critical Components	Input Voltage		
	30 V	800 V	1000 V
Primary Snubber Resistor	49.8	46.0	52.2
InnoSwitch3-AQ	51.7	46.5	49.1
Transformer Core	41.1	44.7	47.7
Transformer Wire	43.8	47.4	50.9
SR FET	41.9	45.9	48.3
Secondary Snubber Resistor	40.6	46.2	49.7
Output Capacitor	38.9	40.5	42.1
Input CMC	41.0	41.4	43.8
Ambient Temperature	26.7	27.5	29.2

Table 9 – Thermals Data at 25 °C at Different Input Voltages.

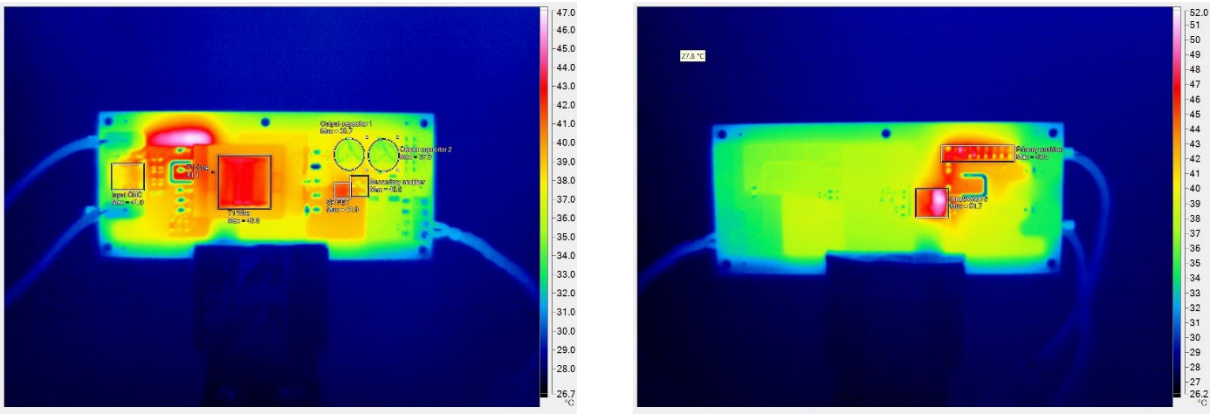


Figure 24 – Top PCB (Left) and Bottom PCB (Right) Thermal Scans at 30 V Input.

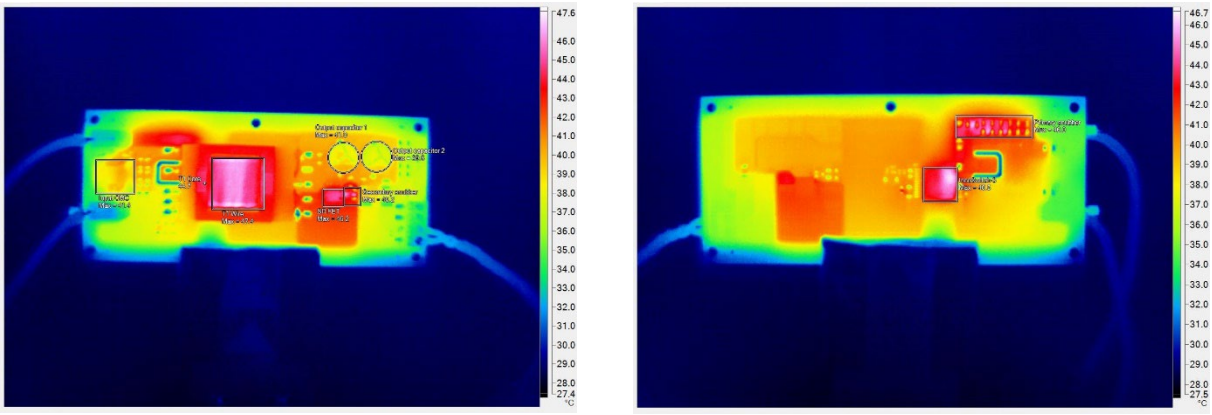


Figure 25 – Top PCB (Left) and Bottom PCB (Right) Thermal Scans at 800 V Input.

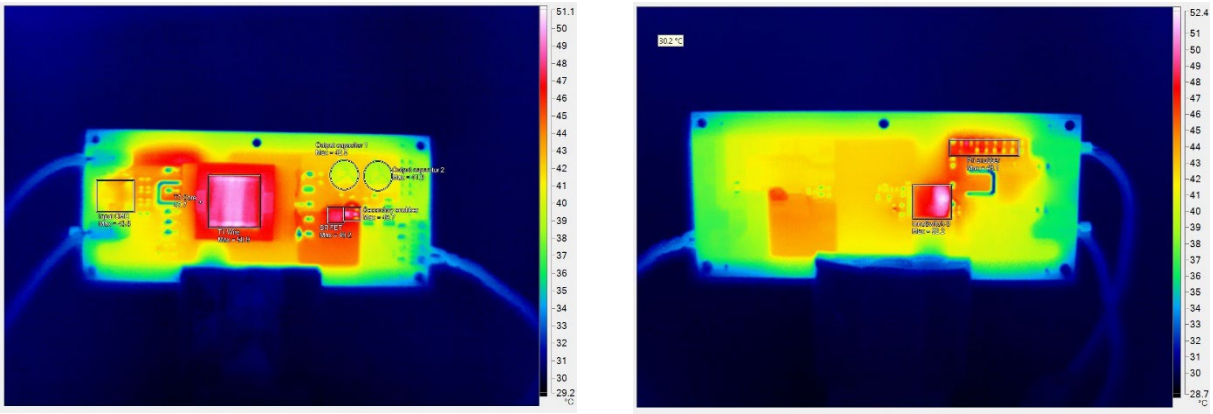


Figure 26 – Top PCB (Left) and Bottom PCB (Right) Thermal Scans at 1000 V Input.

11 Waveforms

11.1 *Start-Up Waveforms*

11.1.1 25 °C Ambient Temperature

The following measurements were taken by hot plugging-in the unit under test to a DC link capacitor fully charged[5] to a test input voltage of HV+.

11.1.1.1 Output Voltage and Current[6,7]

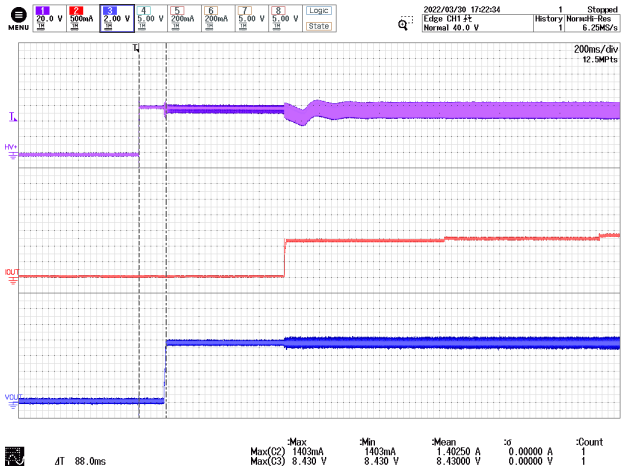


Figure 27 – Output Voltage and Current.
60 V_{DC}, 1.333 A Load.
CH1: HV+, 20 V / div.
CH2: I_{OUT}, 500 mA / div.
CH3: V_{OUT}, 2 V / div.
Time: 200 ms / div.

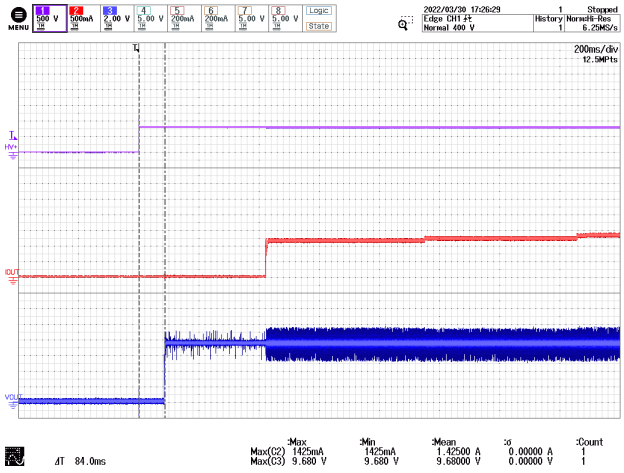


Figure 28 – Output Voltage and Current.
800 V_{DC}, 1.333 A Load.
CH1: HV+, 500 V / div.
CH2: I_{OUT}, 500 mA / div.
CH3: V_{OUT}, 2 V / div.
Time: 200 ms / div.

[5] Inrush current was limited by adding a 10 Ω series resistor between the DC link capacitor and the unit under test.
[6] Voltage dip on the HV+ waveform is due to the effective line impedance from the DC link capacitor to the unit under test.
[7] The instances of small step increase seen on the I_{OUT} waveform is due to the CR (Constant Resistance) mode response of the electronic load. The delay between V_{OUT} and I_{OUT} rising edge is also due to the electronic load response.

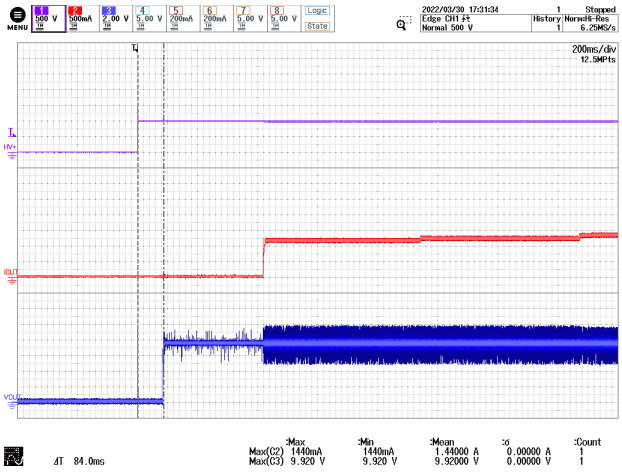


Figure 29 – Output Voltage and Current.
1000 V_{DC}, 1.333 A Load.
CH1: HV+, 500 V / div.
CH2: I_{OUT}, 500 mA / div.
CH3: V_{OUT}, 2 V / div.
Time: 200 ms / div.

11.1.1.2 InnoSwitch3-AQ Drain Voltage and Current[8,9]

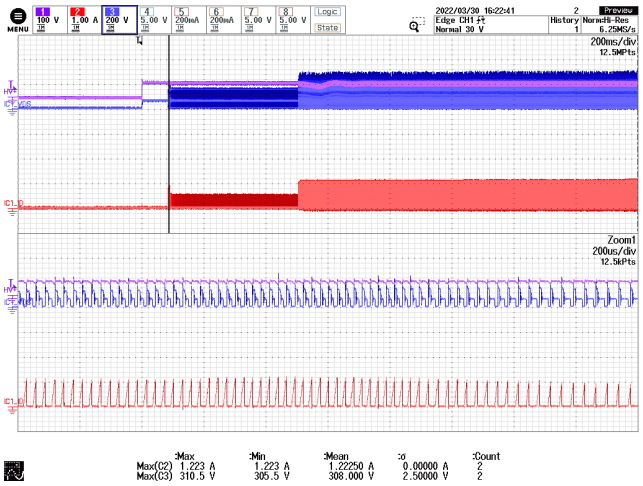


Figure 30 – INN3947CQ Drain Voltage and Current.
60 V_{DC}, 1.333 A Load.
CH1: HV+, 100 V / div.
CH2: I_D, 1 A / div.
CH3: V_{DS}, 200 V / div.
Time: 200 ms / div.

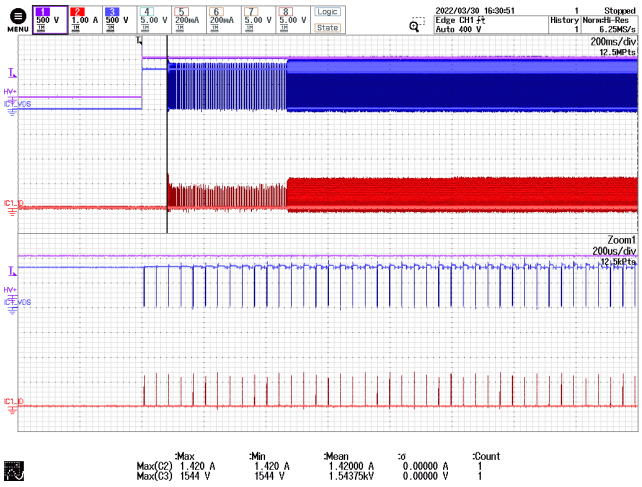


Figure 31 – INN3947CQ Drain Voltage and Current.
800 V_{DC}, 1.333 A Load.
CH1: HV+, 500 V / div.
CH2: I_D, 1 A / div.
CH3: V_{DS}, 500 V / div.
Time: 200 ms / div.

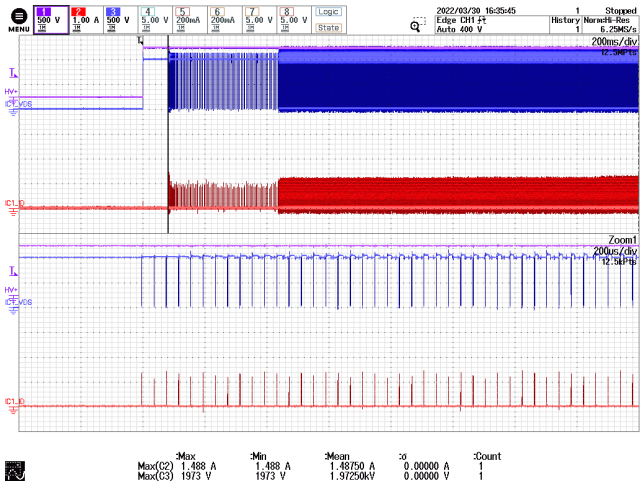


Figure 32 – INN3947CQ Drain Voltage and Current.
1000 V_{DC}, 1.333 A Load.
CH1: HV+, 500 V / div.
CH2: I_D, 1 A / div.
CH3: V_{DS}, 500 V / div.
Time: 200 ms / div.

[8] The time between when HV+ is turned on and the InnoSwitch starts switching is due to the "Wait and Listen" period of the InnoSwitch.
[9] The change in the switching frequency of the InnoSwitch is due to the CR (Constant Resistance) mode response of the electronic load.

11.1.1.3 SR FET Drain Voltage and Current[10,11]

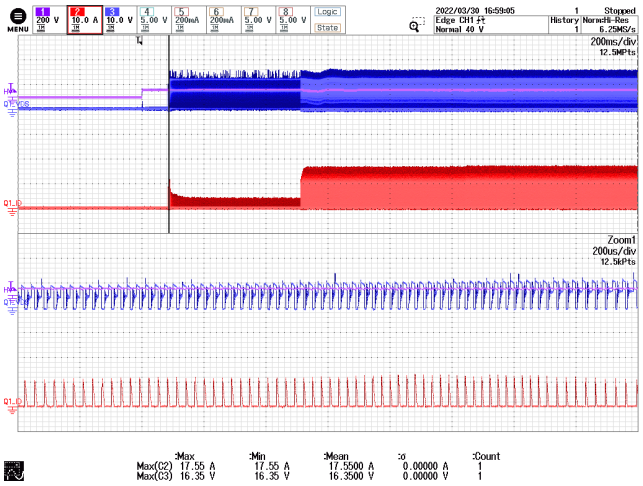


Figure 33 – SR FET Drain Voltage and Current.
60 V_{DC}, 1.333 A Load.
CH1: HV+, 200 V / div.
CH2: I_D, 10 A / div.
CH3: V_{DS}, 10 V / div.
Time: 200 ms / div.

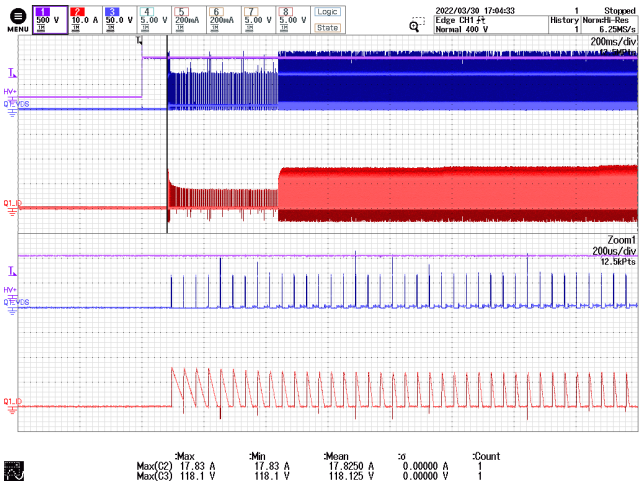


Figure 34 – SR FET Drain Voltage and Current.
800 V_{DC}, 1.333 A Load.
CH1: HV+, 500 V / div.
CH2: I_D, 10 A / div.
CH3: V_{DS}, 50 V / div.
Time: 200 ms / div.

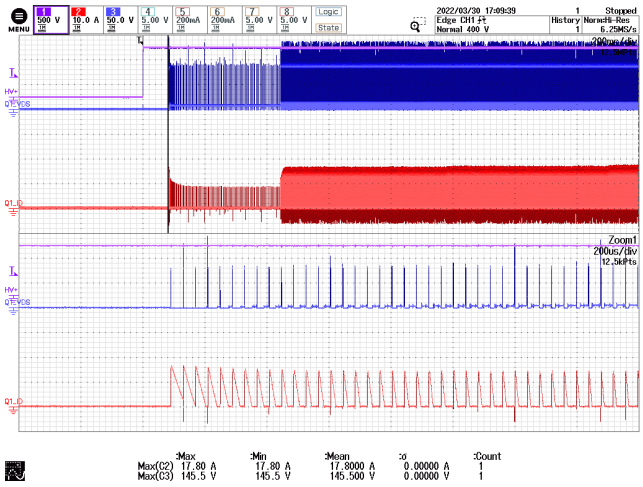


Figure 35 – SR FET Drain Voltage and Current.
1000 V_{DC}, 1.333 A Load.
CH1: HV+, 500 V / div.
CH2: I_D, 10 A / div.
CH3: V_{DS}, 50 V / div.
Time: 200 ms / div.

[10] The time between when HV+ is turned on and the SR FET starts switching is due to the "Wait and Listen" period of the InnoSwitch.
[11] The change in the switching frequency of the SR FET is due to the CR (Constant Resistance) mode response of the electronic load.

11.1.2 - 40 °C Ambient Temperature

11.1.2.1 Output Voltage and Current[12,13]

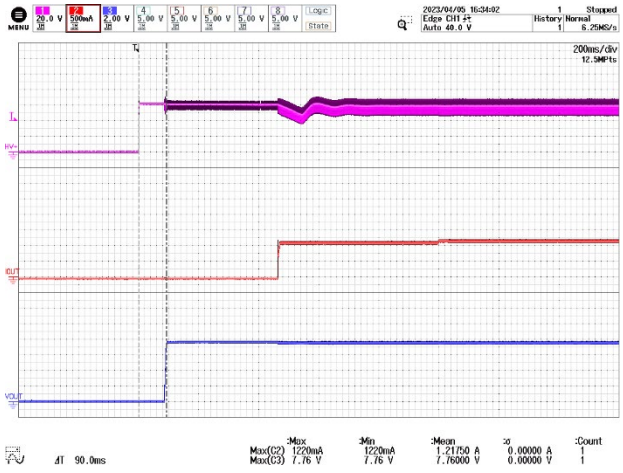


Figure 36 – Output Voltage and Current.
60 V_{DC}, 1.333 A Load.
CH1: HV+, 20 V / div.
CH2: I_{OUT}, 500 mA / div.
CH3: V_{OUT}, 2 V / div.
Time: 200 ms / div.

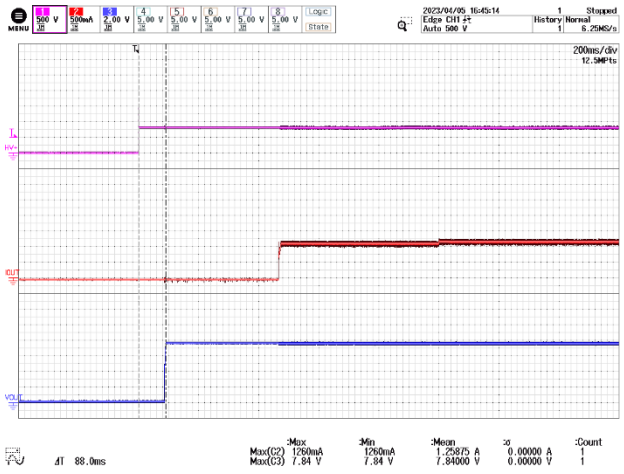


Figure 37 – Output Voltage and Current.
800 V_{DC}, 1.333 A Load.
CH1: HV+, 500 V / div.
CH2: I_{OUT}, 500 mA / div.
CH3: V_{OUT}, 2 V / div.
Time: 200 ms / div.

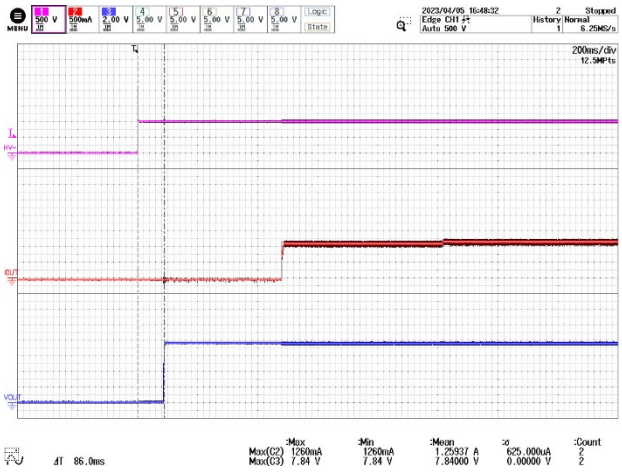


Figure 38 – Output Voltage and Current.
1000 V_{DC}, 1.333 A Load.
CH1: HV+, 500 V / div.
CH2: I_{OUT}, 500 mA / div.
CH3: V_{OUT}, 2 V / div.
Time: 200 ms / div.

[12] Voltage dip on the HV+ waveform is due to the effective line impedance from the DC link capacitor to the unit under test.
[13] The instance of small step increase seen on the I_{OUT} waveform is due to the CR (Constant Resistance) mode response of the electronic load. The delay between V_{OUT} and I_{OUT} rising edge is also due to the electronic load response.

11.1.2.2 InnoSwitch3-AQ Drain Voltage and Current[14,15]

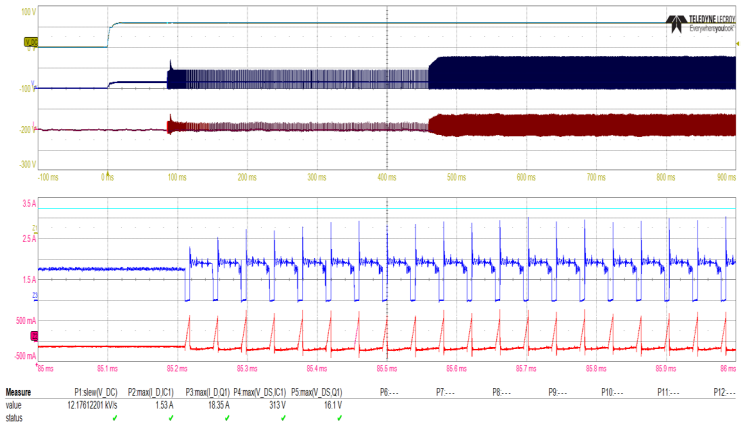


Figure 39 – INN3947CQ Drain Voltage and Current.
60 V_{DC}, 1.333 A Load.
CH1: HV+, 50 V / div.
CH2: I_D, 500 mA / div.
CH3: V_{DS}, 150 V / div.
Time: 100 ms / div.

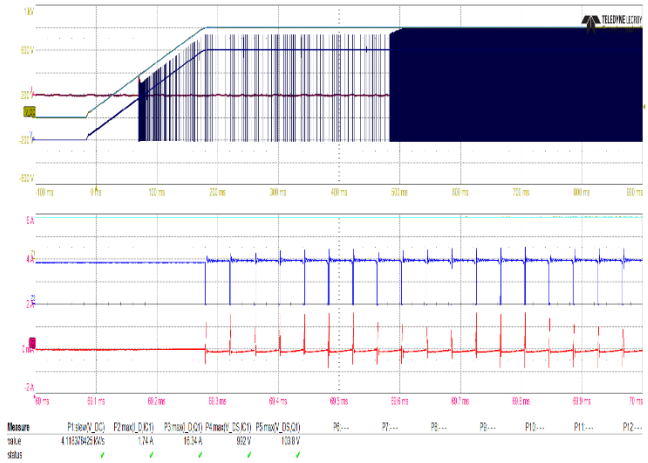


Figure 40 – INN3947CQ Drain Voltage and Current.
800 V_{DC}, 1.333 A Load.
CH1: HV+, 200 V / div.
CH2: I_D, 2 A / div.
CH3: V_{DS}, 200 V / div.
Time: 100 ms / div.

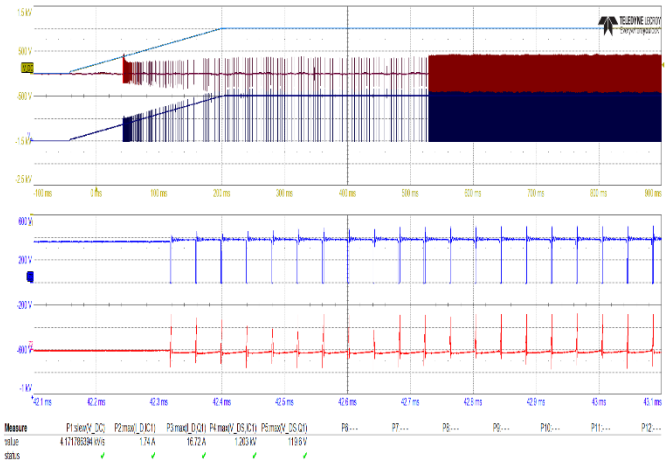


Figure 41 – INN3947CQ Drain Voltage and Current.
1000 V_{DC}, 1.333 A Load.
CH1: HV+, 500 V / div.
CH2: I_D, 1 A / div.
CH3: V_{DS}, 500 V / div.
Time: 100 ms / div.

[14] The time between when HV+ is turned on and the InnoSwitch starts switching is due to the "Wait and Listen" period of the InnoSwitch.
[15] The change in the switching frequency of the InnoSwitch is due to the CR (Constant Resistance) mode response of the electronic load.

11.1.2.3 SR FET Drain Voltage and Current[16,17]

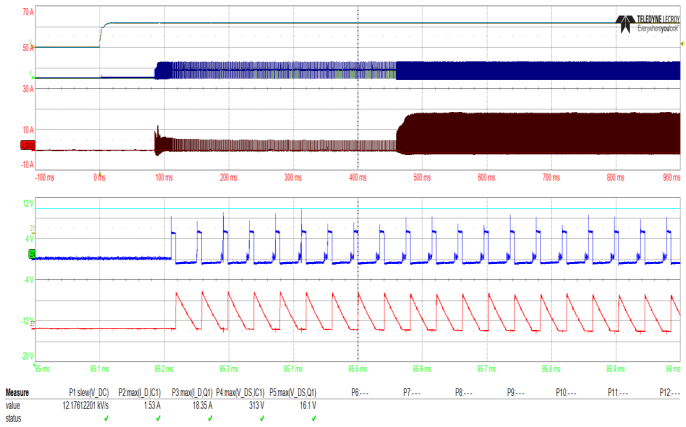


Figure 42 – SR FET Drain Voltage and Current.
60 V_{DC}, 1.333 A Load.
CH1: HV+, 20 V / div.
CH2: I_D, 5 A / div.
CH3: V_{DS}, 10 V / div.
Time: 100 ms / div.

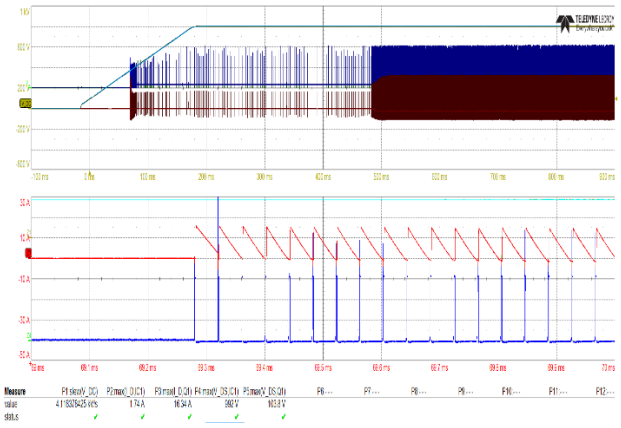


Figure 43 – SR FET Drain Voltage and Current.
800 V_{DC}, 1.333 A Load.
CH1: HV+, 200 V / div.
CH2: I_D, 5 A / div.
CH3: V_{DS}, 50 V / div.
Time: 100 ms / div.

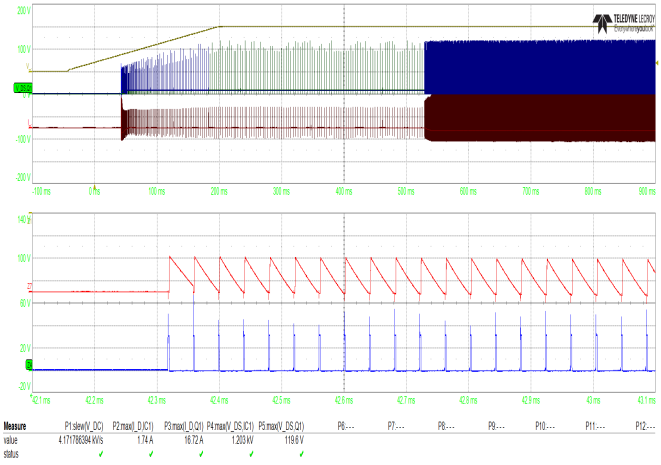


Figure 44 – SR FET Drain Voltage and Current.
1000 V_{DC}, 1.333 A Load.
CH1: HV+, 500 V / div.
CH2: I_D, 10 A / div.
CH3: V_{DS}, 50 V / div.
Time: 100 ms / div.

[16] The time between when HV+ is turned on and the SR FET starts switching is due to the "Wait and Listen" function of the InnoSwitch.
[17] The change in the switching frequency of the SR FET is due to the CR (Constant Resistance) mode response of the electronic load.

11.2 *Steady-State Waveforms*

11.2.1 Switching Waveforms at 105 °C Ambient Temperature

11.2.1.1 Normal Operation Component Stress

Steady-State Switching Waveforms 105 °C Ambient, Full Load				
Input	**INN3947CQ**		**18 V SR FET**	
$V_{IN(V)}$	**IC1 $V_{DS(V)}$**	**$V_{STRESS(\%)}$**	**Q1 $V_{DS(V)}$**	**$V_{STRESS(\%)}$**
30	260.5	15.32	19.02	12.68%
60	332	19.53	17.3	11.53%
800	1030	60.59	124	82.67%
1000	1240	72.94	139.3	92.67%

Table 10 – Summary of Critical Component Voltage Stresses at 105 °C Ambient Temperature

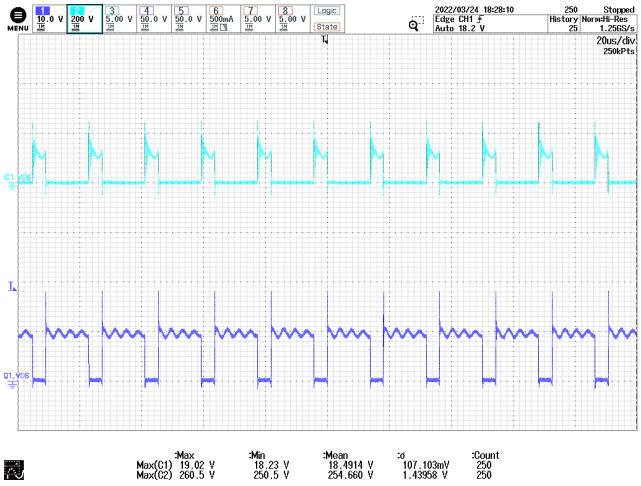


Figure 45 – InnoSwitch3-AQ and SR FET Drain Voltage.
30 V_{DC}, 1.333 A Load, 105 °C Ambient.
CH1: $V_{Q1,VDS}$, 10 V / div.
CH2: $V_{IC1,VDS}$, 200 V / div.
Time: 20 µs / div.

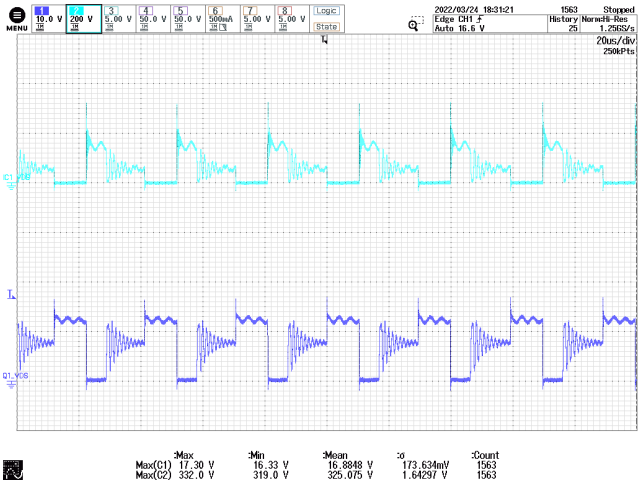


Figure 46 – InnoSwitch3-AQ and SR FET Drain Voltage.
60 V_{DC}, 1.333 A Load, 105 °C Ambient.
CH1: $V_{Q1,VDS}$, 10 V / div.
CH2: $V_{IC1,VDS}$, 200 V / div.
Time: 20 µs / div.

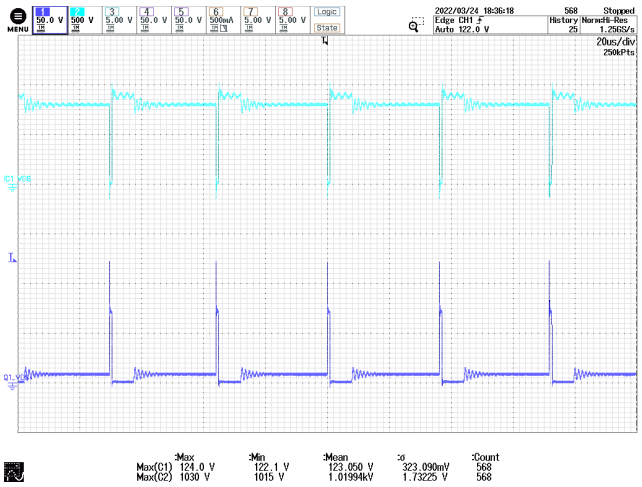


Figure 47 – InnoSwitch3-AQ and SR FET Drain Voltage. 800 V_{DC}, 1.333 A Load, 105 °C Ambient.
CH1: $V_{Q1,VDS}$, 50 V / div.
CH2: $V_{IC1,VDS}$, 500 V / div.
Time: 20 µs / div.

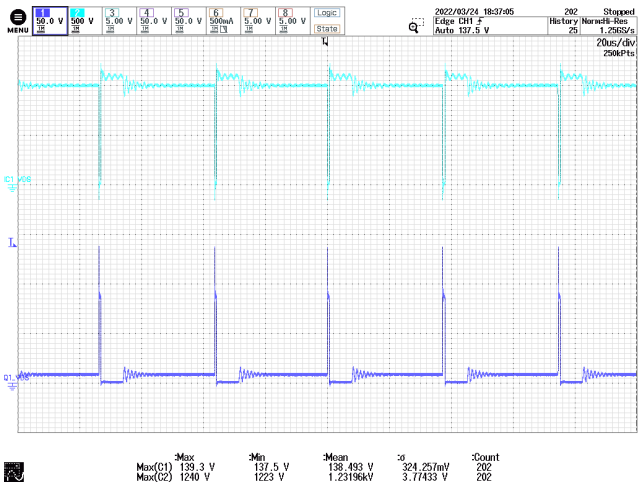


Figure 48 – InnoSwitch™3-AQ and SR FET Drain Voltage. 1000 V_{DC}, 1.333 A Load, 105 °C Ambient.
CH1: $V_{Q1,VDS}$, 50 V / div.
CH2: $V_{IC1,VDS}$, 500 V / div.
Time: 20 µs / div.

11.2.1.2 Short-Circuit Response

The unit is tested by applying output short circuit during normal working conditions and then removing the short circuit to see if the unit will recover and operate normally. The expected response during short-circuit is for the unit to go to AR (auto restart) mode.

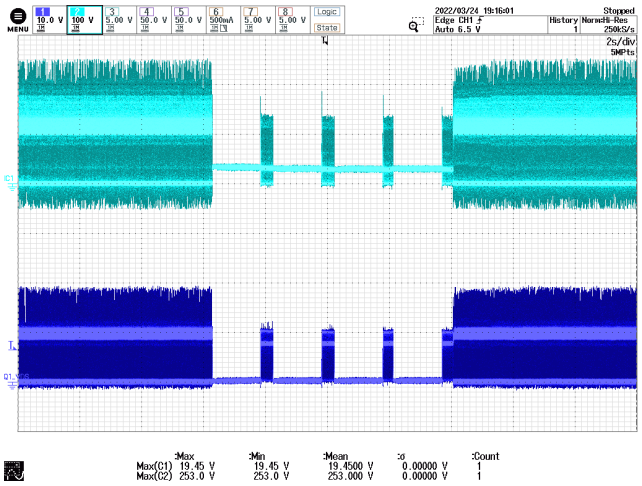


Figure 49 – InnoSwitch3-AQ and SR FET Drain Voltage. 30 V_{DC}, Full Load-Short-Full Load, 105 °C Ambient.
CH1: $V_{Q1,VDS}$, 10 V / div.
CH2: $V_{IC1,VDS}$, 100 V / div.
Time: 20 µs / div.

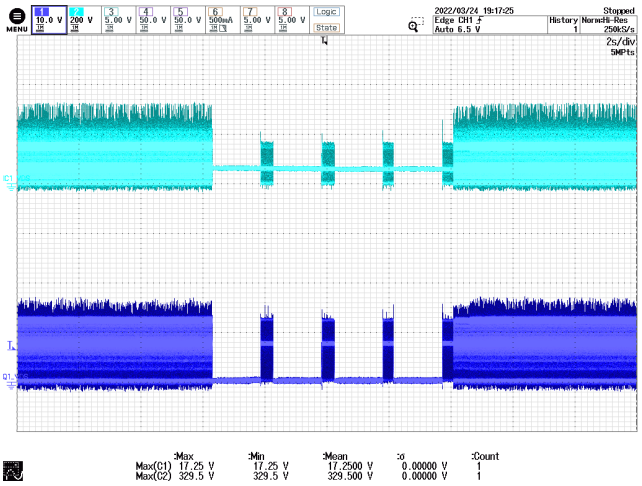


Figure 50 – InnoSwitch3-AQ and SR FET Drain Voltage. 60 V_{DC}, Full Load-Short-Full Load, 105 °C Ambient.
CH1: $V_{Q1,VDS}$, 10 V / div.
CH2: $V_{IC1,VDS}$, 200 V / div.
Time: 20 µs / div.

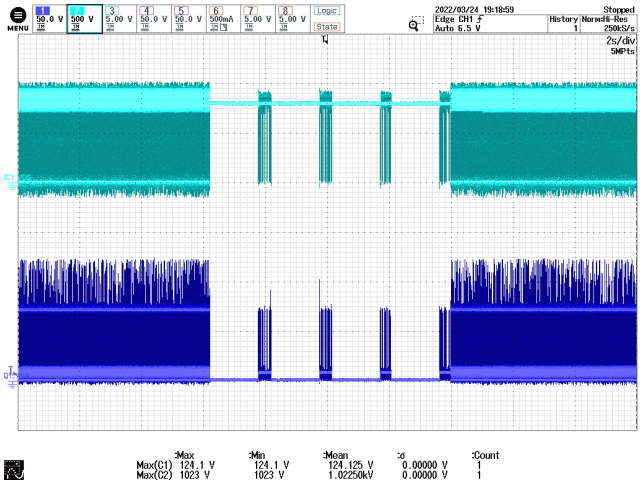


Figure 51 – InnoSwitch3-AQ and SR FET Drain voltage. 800 V_{DC}, Full Load-Short-Full Load, 105 °C ambient.
CH1: $V_{Q1,VDS}$, 50 V / div.
CH2: $V_{IC1,VDS}$, 500 V / div.
Time: 20 µs / div.

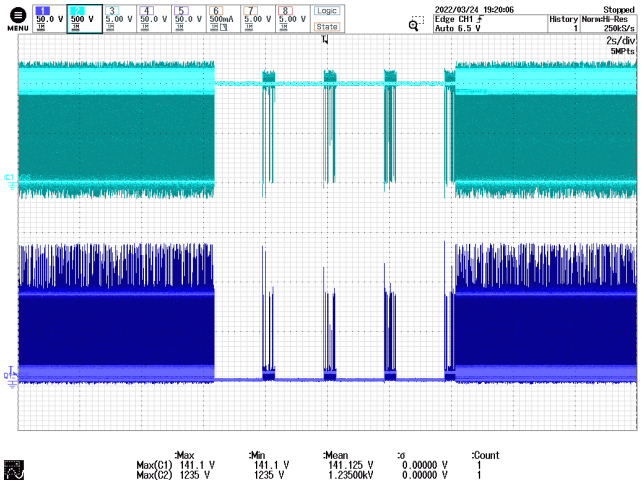


Figure 52 – InnoSwitch3-AQ and SR FET Drain voltage. 1000 V_{DC}, Full Load-Short-Full Load, 105 °C ambient.
CH1: $V_{Q1,VDS}$, 50 V / div.
CH2: $V_{IC1,VDS}$, 500 V / div.
Time: 20 µs / div.

11.2.2 Switching Waveforms at 25 °C Ambient Temperature

11.2.2.1 InnoSwitch3-AQ Drain Voltage and Current

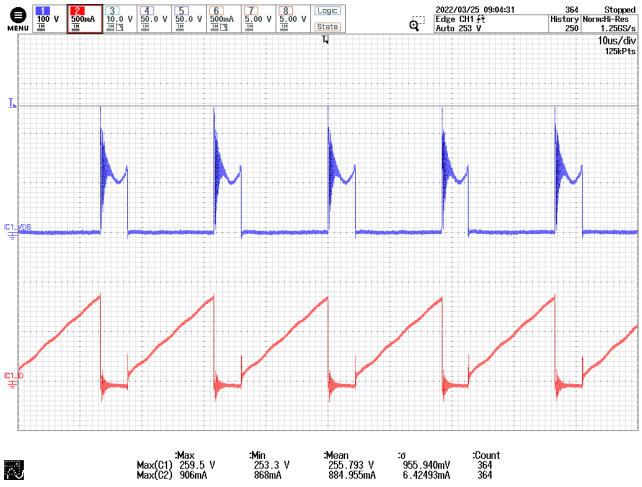


Figure 53 – INN3947CQ Drain Voltage and Current. 30 V_{DC}, 1.333 A Load.
CH1: V_{DS}, 100 V / div.
CH2: I_D, 500 mA / div.
Time: 10 µs / div.

Figure 54 – INN3947CQ Drain Voltage and Current. 60 V_{DC}, 1.333 A Load.
CH1: V_{DS}, 100 V / div.
CH2: I_D, 500 mA / div.
Time: 10 µs / div.

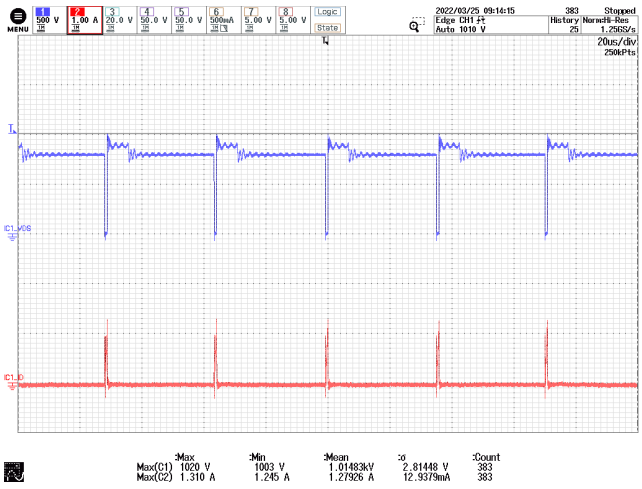


Figure 55 – INN3947CQ Drain Voltage and Current.
800 V_{DC}, 1.333 A Load.
CH1: V_{DS}, 500 V / div.
CH2: I_D, 1 A / div.
Time: 20 µs / div.

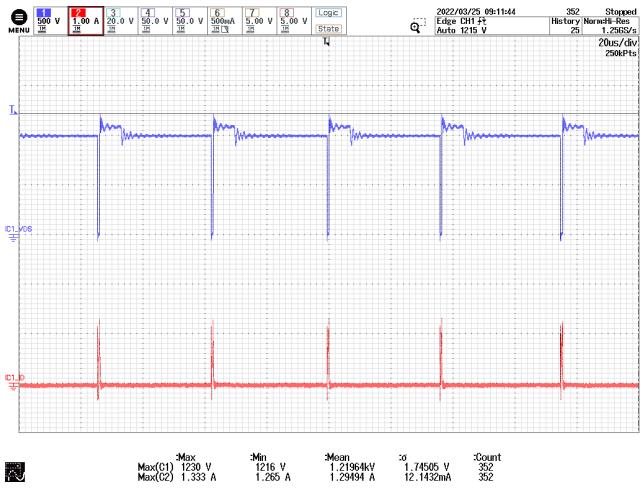


Figure 56 – INN3947CQ Drain Voltage and Current.
1000 V_{DC}, 1.333 A Load.
CH1: V_{DS}, 500 V / div.
CH2: I_D, 1 A / div.
Time: 20 µs / div.

11.2.2.2 SR FET Drain Voltage and Current

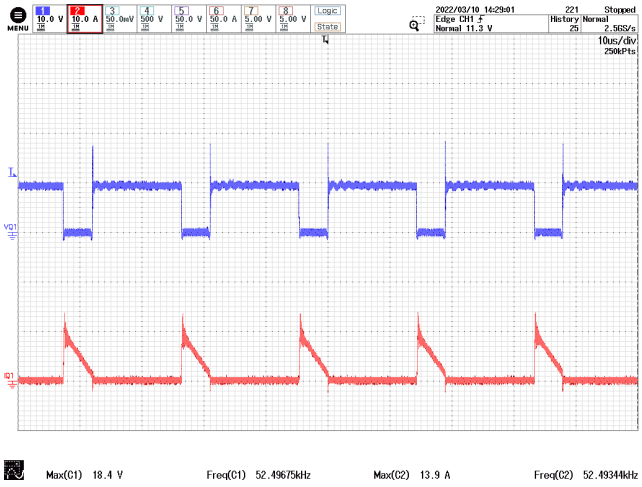


Figure 57 – SR FET Drain Voltage and Current.
30 V_{DC}, 1.333 A Load.
CH1: V_{DS}, 10 V / div.
CH2: I_D, 10 A / div.
Time: 10 µs / div.

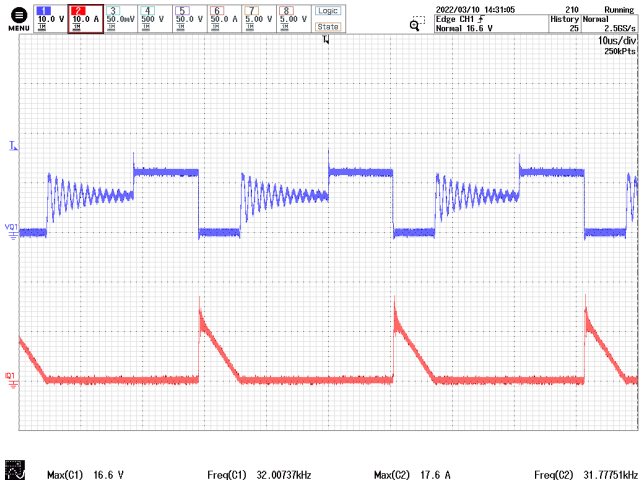


Figure 58 – SR FET Drain Voltage and Current.
60 V_{DC}, 1.333 A Load.
CH1: V_{DS}, 10 V / div.
CH2: I_D, 10 A / div.
Time: 10 µs / div.

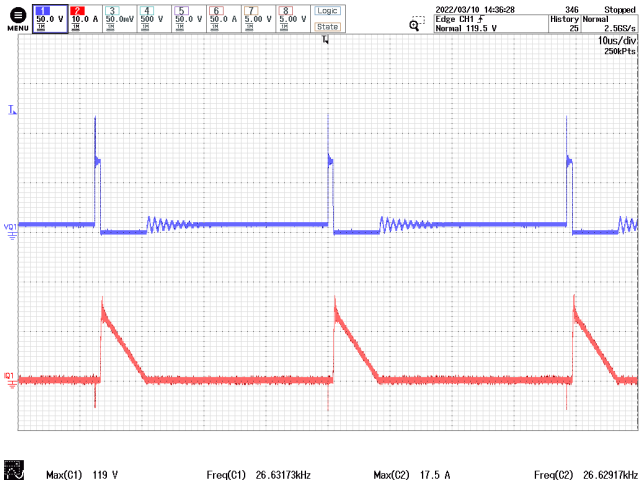


Figure 59 – SR FET Drain Voltage and Current.
800 V_{DC}, 1.333 A Load.
CH1: V_{DS}, 50 V / div.
CH2: I_D, 10 A / div.
Time: 20 µs / div.

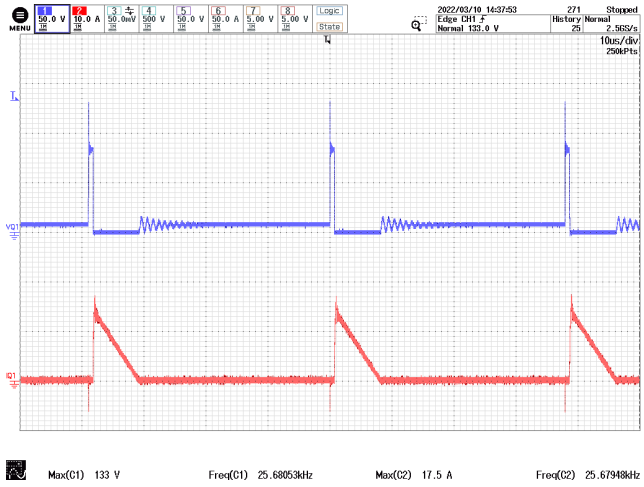


Figure 60 – SR FET Drain Voltage and Current.
1000 V_{DC}, 1.333 A Load.
CH1: V_{DS}, 50 V / div.
CH2: I_D, 10 A / div.
Time: 20 µs / div.

11.3 *Load Transient Response*

Output voltage waveform on the board was captured with dynamic load transient from 0% to 50% and 50% to 100%. The duration for the load states is set to 100 ms and the load slew rate is 100 mA / µs. The test is done at 105 °C ambient temperature.

Dynamic Load Settings	V_{IN} (V)	ΔV_{OUT} (V)	$V_{OUT(MAX)}$ (V)	$V_{OUT(MIN)}$ (V)
0% to 50%	30	0.636	7.50	6.86
	60	0.196	7.52	7.31
	400	0.192	7.54	7.34
	800	0.143	7.52	7.38
	1000	0.235	7.59	7.35
50% to 100%	30	0.479	7.49	7.01
	60	0.233	7.52	7.29
	400	0.264	7.57	7.30
	800	0.271	7.58	7.30
	1000	0.273	7.59	7.31

Table 11 – Load Transient Response.

11.3.1 0% to 50%

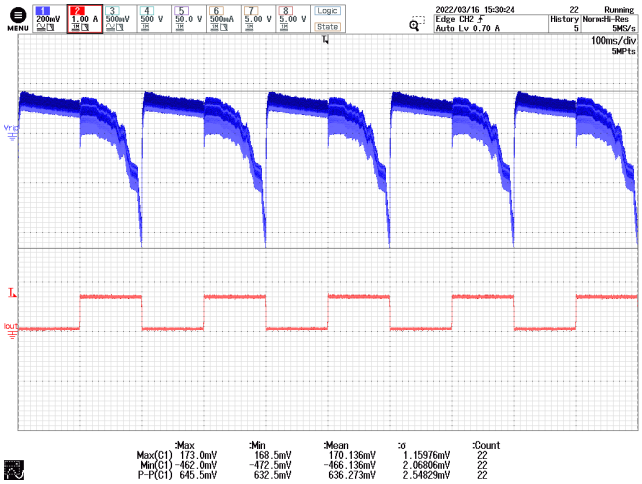


Figure 61 – Output Voltage and Current.
30 V_{DC}, 0% to 50% Transient Load,
105 °C Ambient.
CH1: V_{OUT}, 200 mV / div.
CH2: I_{OUT}, 1 A / div.
Time: 100 ms / div.
ΔV = 636.27 mV.

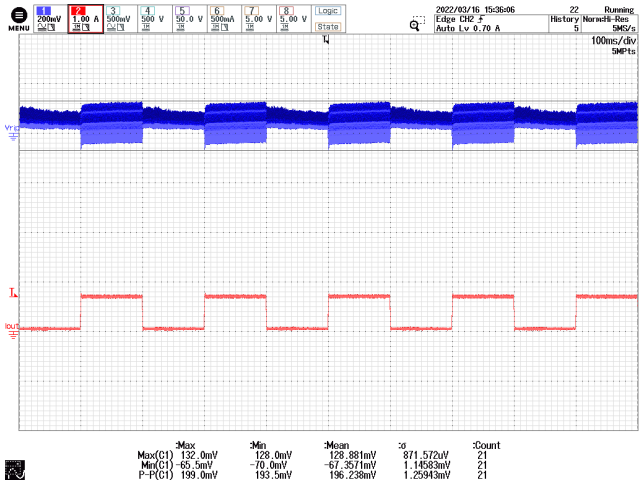


Figure 62 – Output Voltage and Current.
60 V_{DC}, 0% to 50% Transient Load,
105 °C Ambient.
CH1: V_{OUT}, 200 mV / div.
CH2: I_{OUT}, 1 A / div.
Time: 100 ms / div.
ΔV = 196.24 mV.

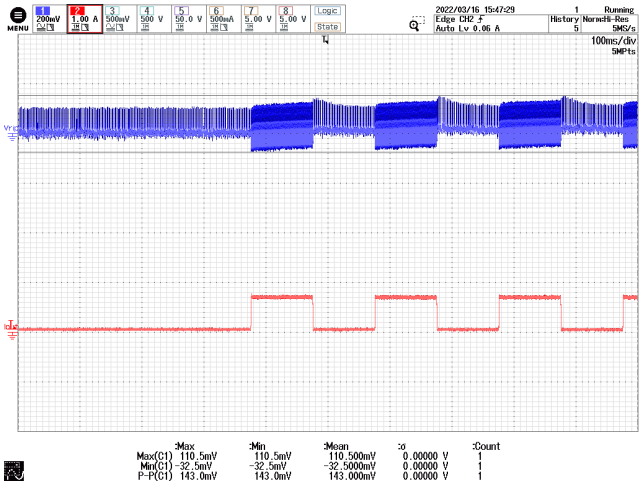


Figure 63 – Output Voltage and Current.
800 V_{DC}, 0% to 50% Transient Load,
105 °C Ambient.
CH1: V_{OUT}, 200 mV / div.
CH2: I_{OUT}, 1 A / div.
Time: 100 ms / div.
ΔV = 143 mV.

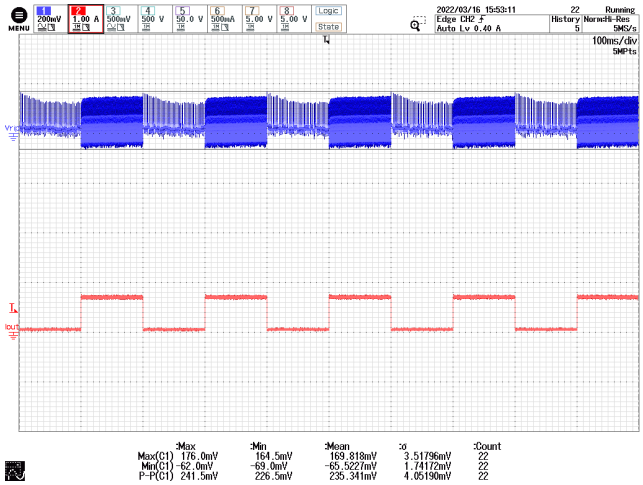


Figure 64 – Output Voltage and Current.
1000 V_{DC}, 0% to 50% Transient Load,
105 °C Ambient.
CH1: V_{OUT}, 200 mV / div.
CH2: I_{OUT}, 1 A / div.
Time: 100 ms / div.
ΔV = 235.34 mV.

11.3.2 50% to 100%

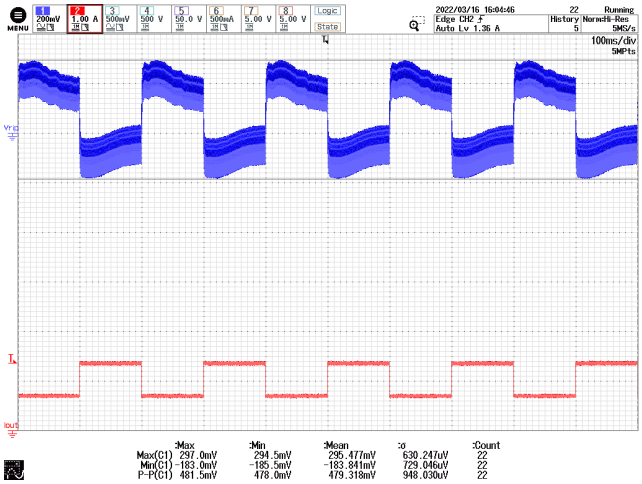


Figure 65 – Output Voltage and Current.
30 V_{DC}, 0% to 50% Transient Load,
105 °C Ambient.
CH1: V_{OUT}, 200 mV / div.
CH2: I_{OUT}, 1 A / div.
Time: 100 ms / div.
ΔV = 479.32 mV.

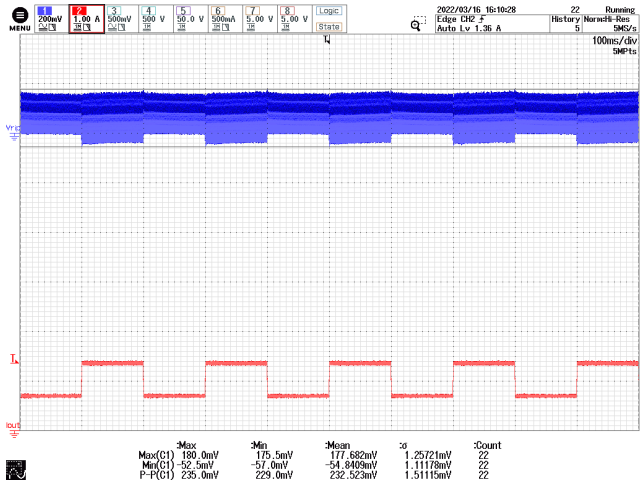


Figure 66 – Output Voltage and Current.
60 V_{DC}, 0% to 50% Transient Load,
105 °C Ambient.
CH1: V_{OUT}, 200 mV / div.
CH2: I_{OUT}, 1 A / div.
Time: 100 ms / div.
ΔV = 232.52 mV.

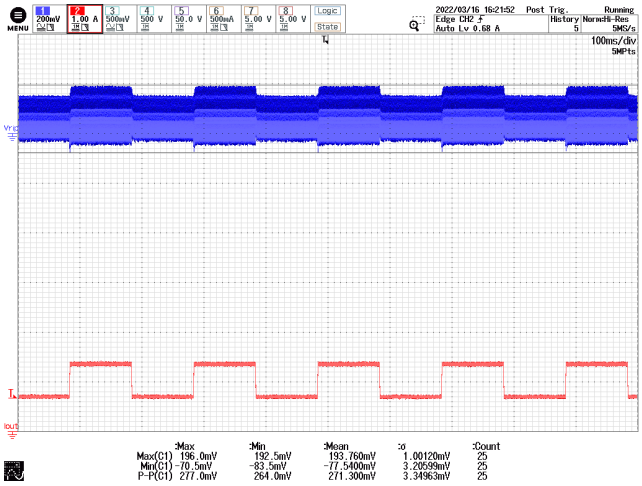


Figure 67 – Output Voltage and Current.
800 V_{DC}, 0% to 50% Transient Load,
105 °C Ambient.
CH1: V_{OUT}, 200 mV / div.
CH2: I_{OUT}, 1 A / div.
Time: 100 ms / div.
ΔV = 271.3 mV.

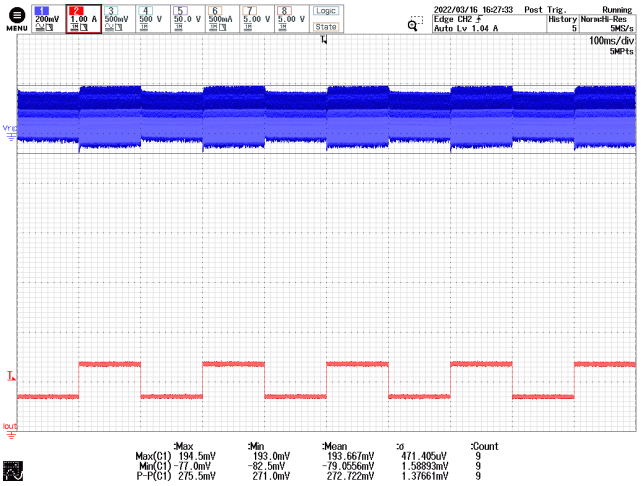


Figure 68 – Output Voltage and Current
1000 V_{DC}, 0% to 50% Transient Load,
105 °C Ambient.
CH1: V_{OUT}, 200 mV / div.
CH2: I_{OUT}, 1 A / div.
Time: 100 ms / div.
ΔV = 272.72 mV.

11.4 *Output Ripple Measurements*

11.4.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized to reduce spurious signals due to pick-up. Details of the probe modification are provided in Figure 69 and Figure 70 below.

A CT2708 probe adapter is affixed with a 1 μF / 50 V ceramic capacitor placed in parallel across the probe tip. A twisted pair of wires kept as short as possible is soldered directly to the probe and the output terminals.

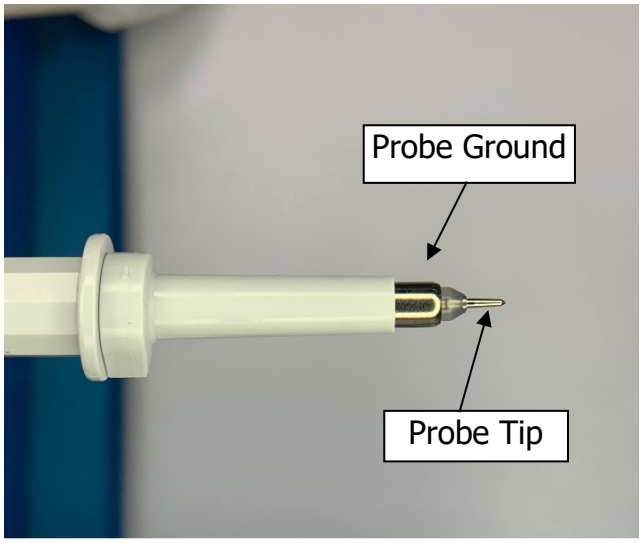


Figure 69 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed.)

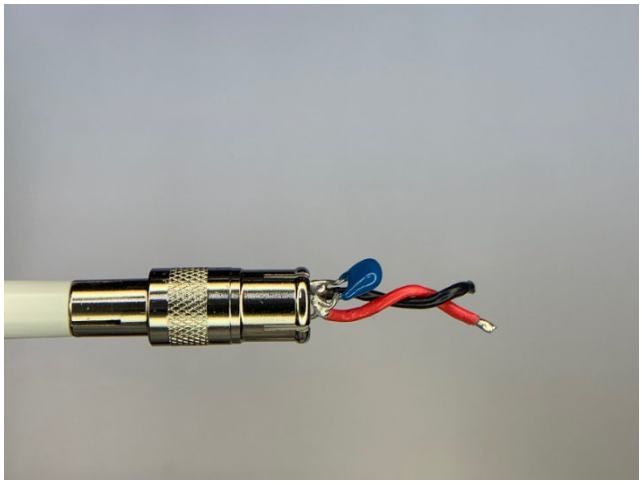


Figure 70 – Oscilloscope Probe with Cal Test CT2708 BNC Adapter. (Modified with Wires for Ripple Measurement, and a Parallel Decoupling Capacitor Added.)

11.4.2 Output Voltage Ripple Waveforms

Output voltage ripple waveform at full load was captured at the output terminals using the ripple measurement probe with decoupling capacitor.

11.4.2.1 Output Voltage Ripple at 105 °C Ambient[18]

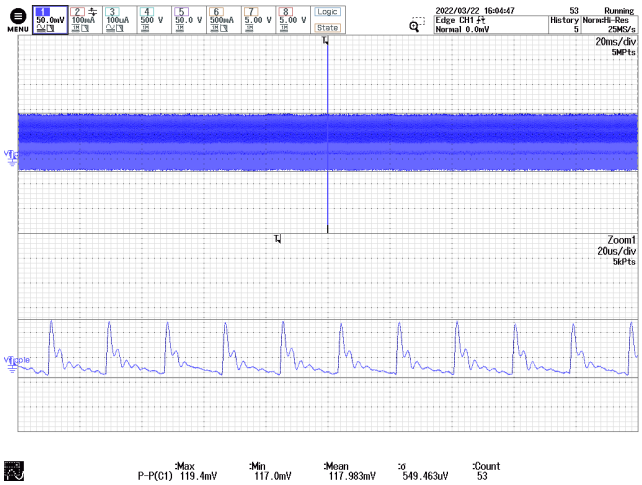


Figure 71 – Output Voltage Ripple.
30 V_{DC}, Full Load, 105 °C Ambient.
CH1: V_{OUT}, 50 mV / div.
Time: 20 ms / div.
V_{RIPPLE} = 119.4 mV.

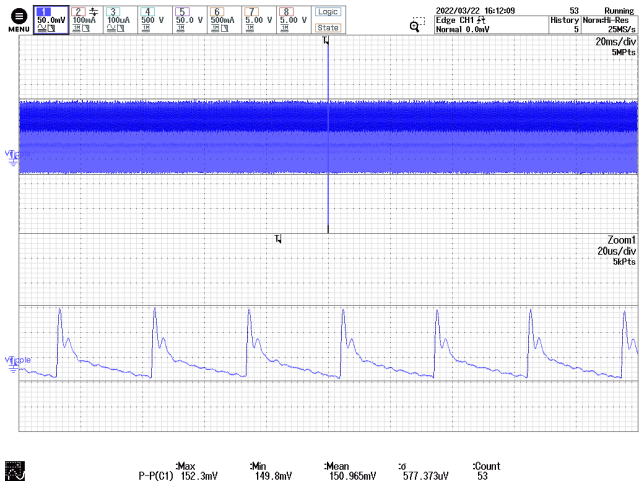


Figure 72 – Output Voltage Ripple.
60 V_{DC}, Full Load, 105 °C Ambient.
CH1: V_{OUT}, 50 mV / div.
Time: 20 ms / div.
V_{RIPPLE} = 152.3 mV.

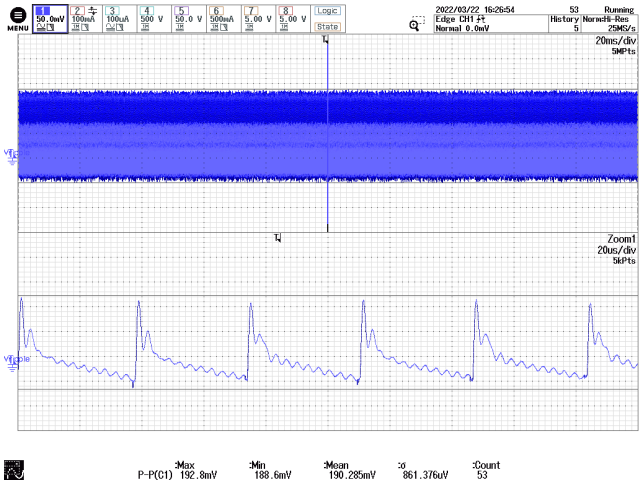


Figure 73 – Output Voltage Ripple.
800 V_{DC}, Full Load, 105 °C Ambient.
CH1: V_{OUT}, 50 mV / div.
Time: 20 ms / div.
V_{RIPPLE} = 192.8 mV.

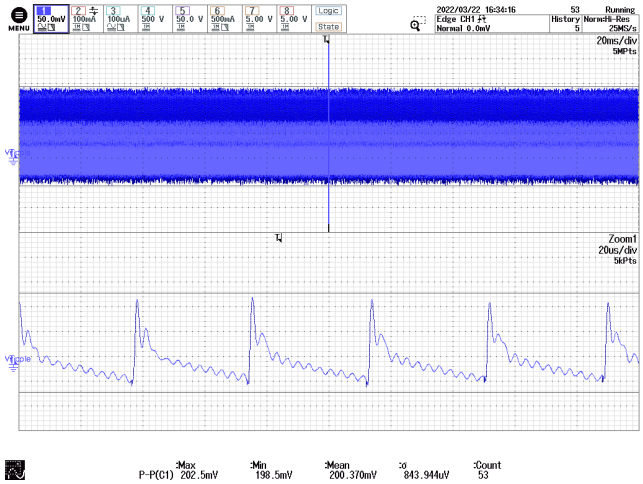


Figure 74 – Output Voltage Ripple.
1000 V_{DC}, Full Load, 105 °C Ambient.
CH1: V_{OUT}, 50 mV / div.
Time: 20 ms / div.
V_{RIPPLE} = 202.5 mV.

[18] Peak-to-peak voltage measurement recorded in each oscilloscope capture is the worst-case ripple which includes both the low frequency and high frequency switching voltage ripple (top portion of each capture).

11.4.2.2 Output Voltage Ripple at 25 °C Ambient[19]

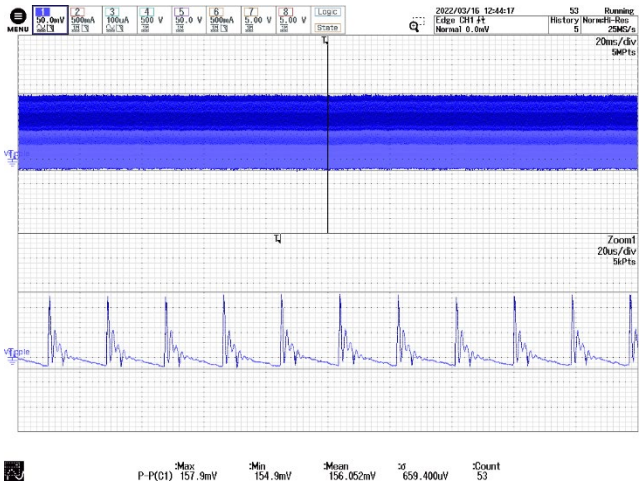


Figure 75 – Output Voltage Ripple.
30 V_{DC}, Full Load, 25 °C Ambient.
CH1: V_{OUT}, 50 mV / div.
Time: 20 ms / div.
V_{RIPPLE} = 157.9 mV.

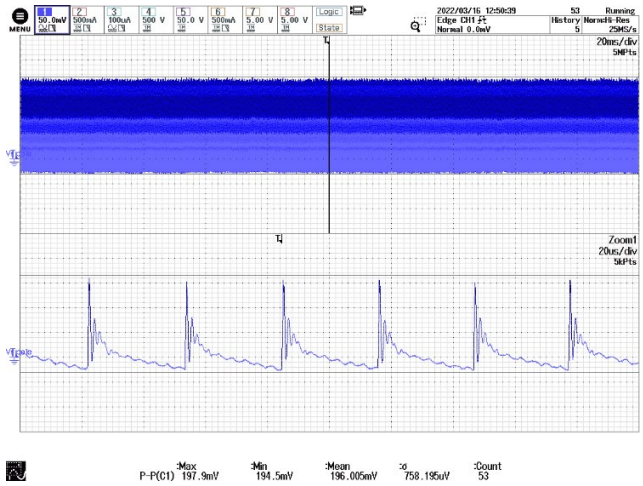


Figure 76 – Output Voltage Ripple.
60 V_{DC}, Full Load, 25 °C Ambient.
CH1: V_{OUT}, 50 mV / div.
Time: 20 ms / div.
V_{RIPPLE} = 197.9 mV.

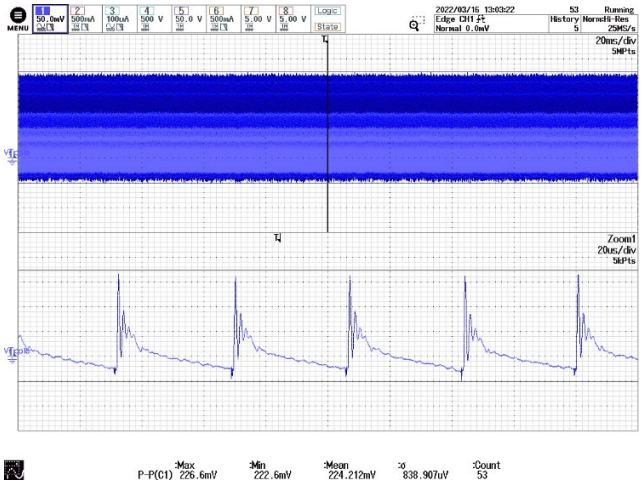


Figure 77 – Output Voltage Ripple.
800 V_{DC}, Full Load, 25 °C Ambient.
CH1: V_{OUT}, 50 mV / div.
Time: 20 ms / div.
V_{RIPPLE} = 226.6 mV.

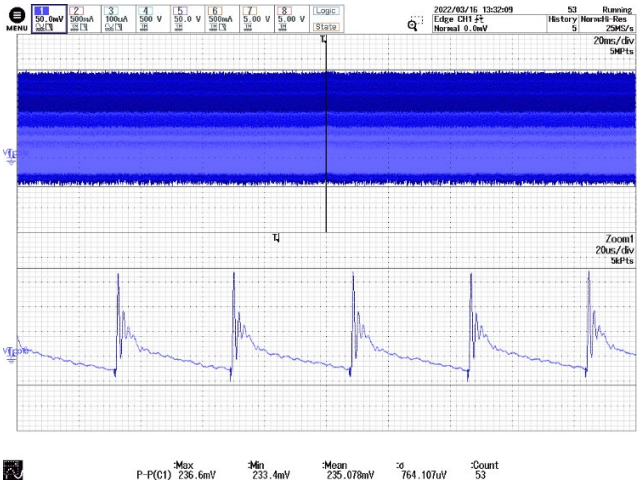


Figure 78 – Output Voltage Ripple.
1000 V_{DC}, Full Load, 25 °C Ambient.
CH1: V_{OUT}, 50 mV / div.
Time: 20 ms / div.
V_{RIPPLE} = 236.6 mV.

[19] Peak-to-peak voltage measurement recorded in each oscilloscope capture is the worst-case ripple which includes both the low frequency and high frequency switching voltage ripple (top portion of each capture).

11.4.2.3 Output Voltage Ripple at -40 °C Ambient[20]

Probe extension using twisted pair wires was implemented for the test performed at -40 °C ambient temperature due to the inaccessibility of the probing point once placed inside the thermal chamber. To compensate for the effects of the probe extension, values shown on the figures below must be increased by 74.66 mV_{PP}[21].

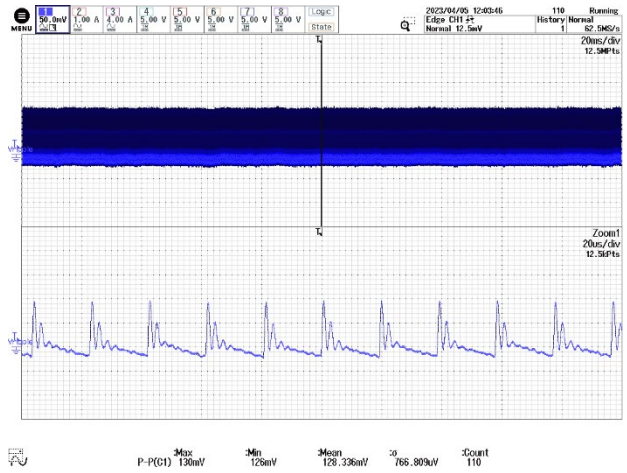


Figure 79 – Output Voltage Ripple.
30 V_{DC}, Full Load, -40 °C Ambient.
CH1: V_{OUT}, 50 mV / div.
Time: 20 ms / div.
V_{RIPPLE} = 130 mV.

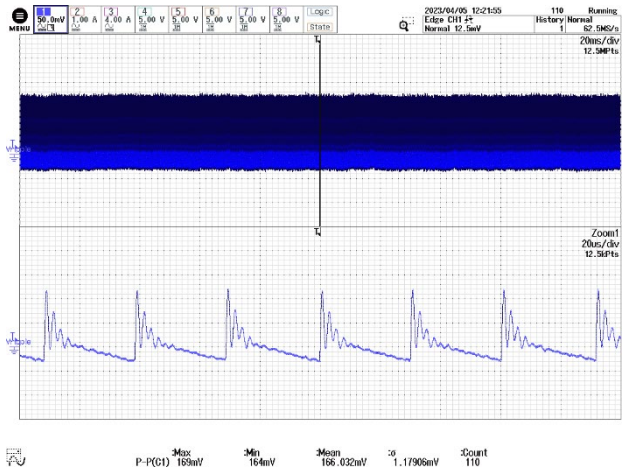


Figure 80 – Output Voltage Ripple.
60 V_{DC}, Full Load, -40 °C Ambient.
CH1: V_{OUT}, 50 mV / div.
Time: 20 ms / div.
V_{RIPPLE} = 169 mV.

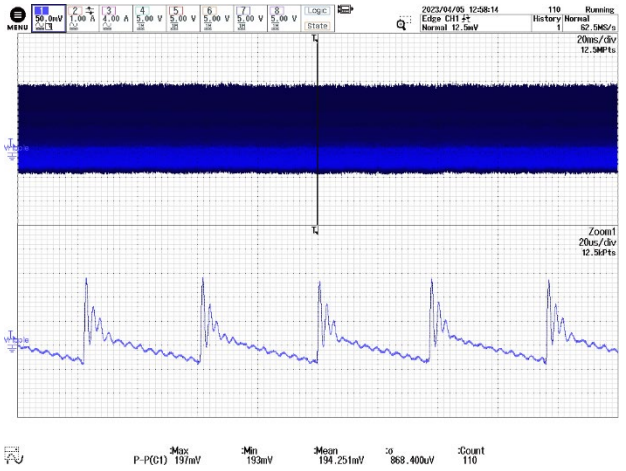


Figure 81 – Output Voltage Ripple.
800 V_{DC}, Full Load, -40 °C Ambient.
CH1: V_{OUT}, 50 mV / div.
Time: 20 ms / div.
V_{RIPPLE} = 197 mV.

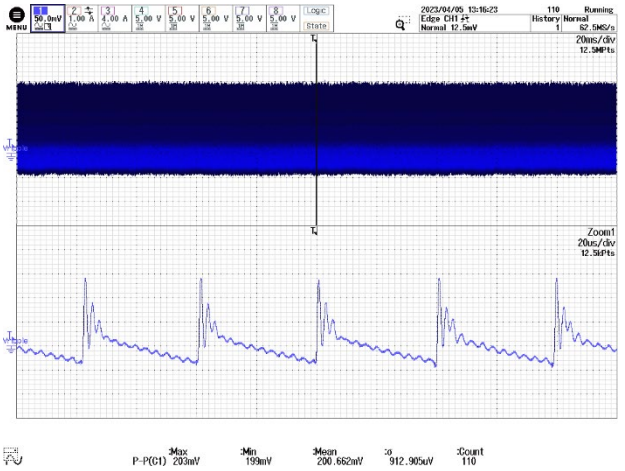


Figure 82 – Output Voltage Ripple.
1000 V_{DC}, Full Load, -40 °C Ambient.
CH1: V_{OUT}, 50 mV / div.
Time: 20 ms / div.
V_{RIPPLE} = 203 mV.

[20] Peak-to-peak voltage measurement recorded in each oscilloscope capture is the worst-case ripple which includes both the low frequency and high frequency switching voltage ripple (top portion of each capture).
[21] 74.66 mV_{PP} is the average value of the difference between the output voltage ripple measurements obtained while using a short and extended probe at 25 °C ambient temperature.

11.4.3 Output Ripple vs. Load

11.4.3.1 Output Ripple at 105 °C Ambient

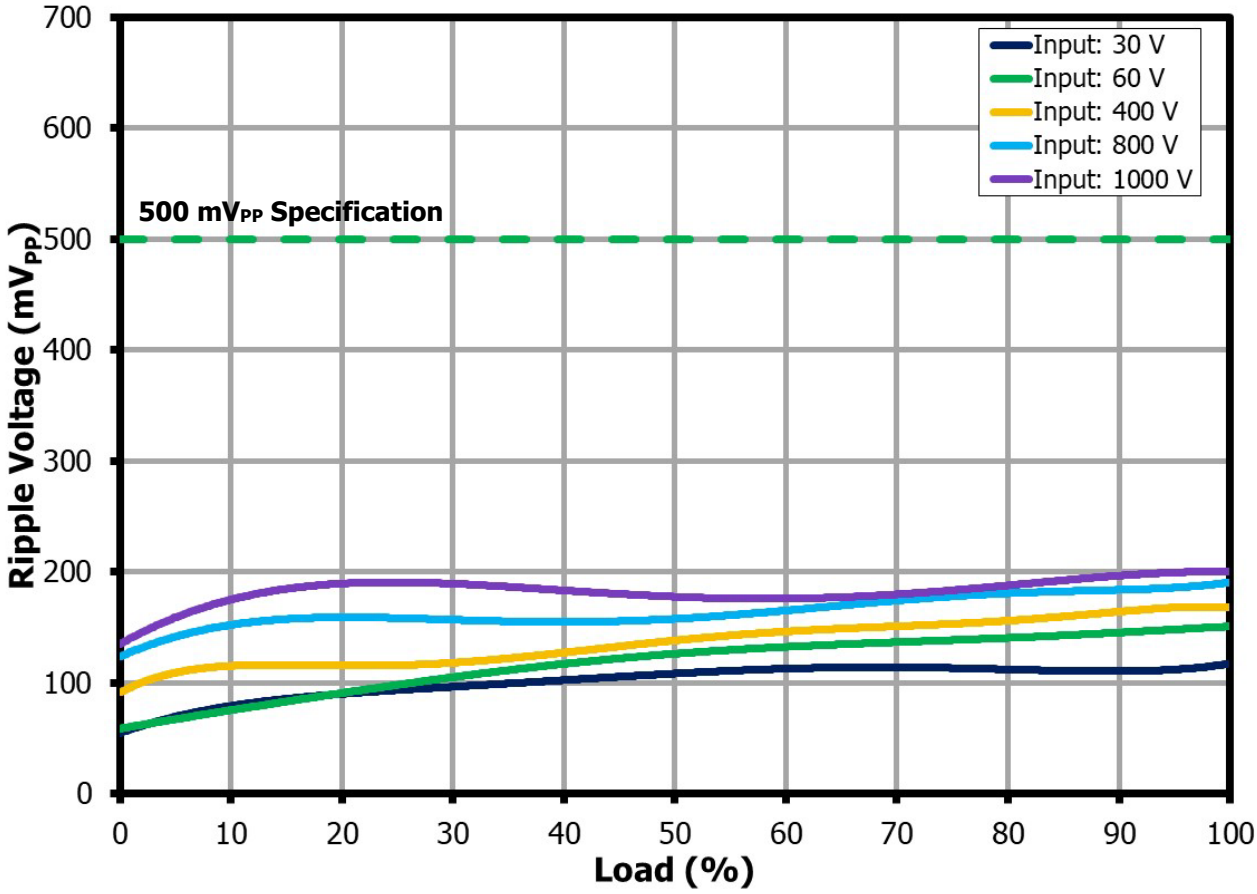


Figure 83 – Output Ripple Voltage (105 °C Ambient).

11.4.3.2 Output Ripple at 25 °C Ambient

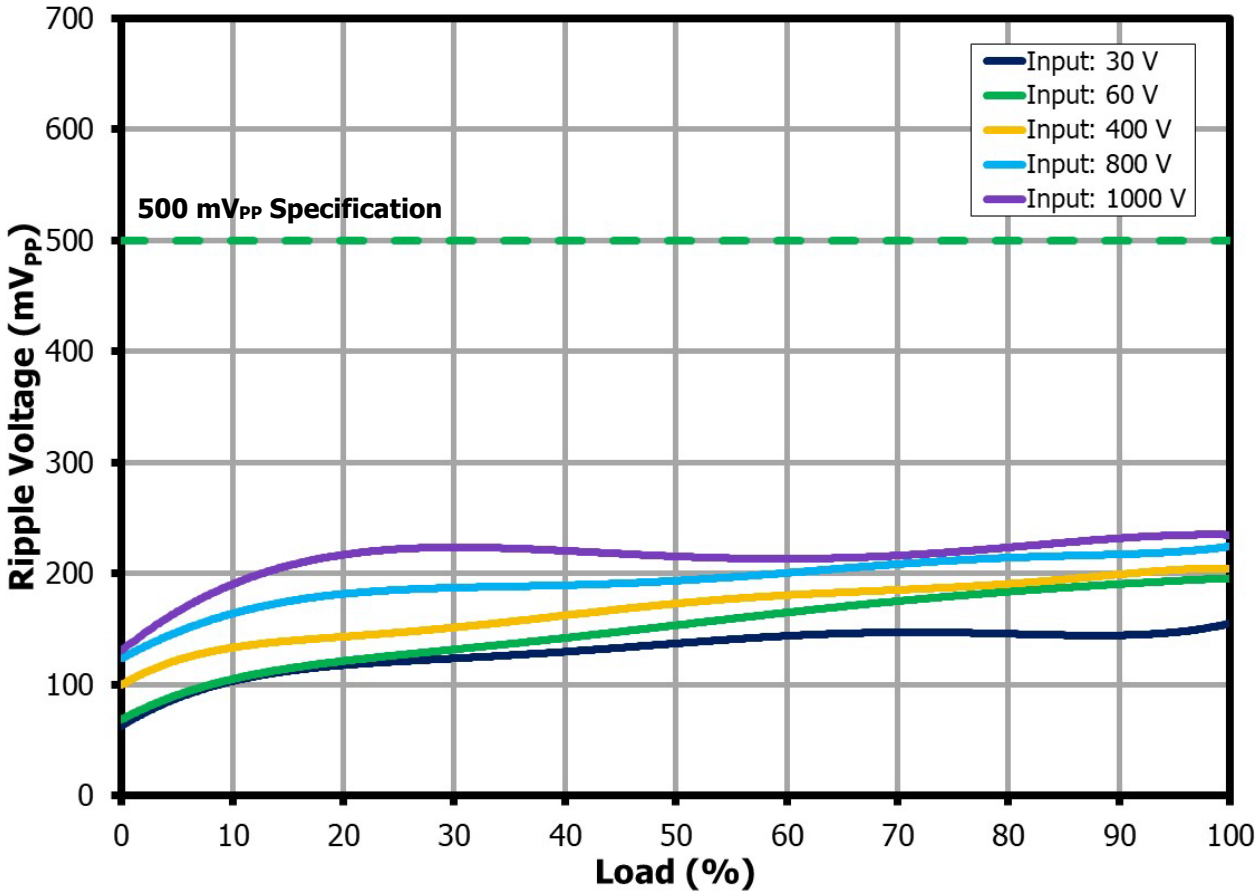


Figure 84 – Output Ripple Voltage (25 °C Ambient).

11.4.3.3 Output Ripple at -40 °C Ambient

Output voltage ripple data at -40 °C ambient temperature shown below includes the 74.66 mV_{PP}[22] offset to compensate for the effect the probe extensions had on the voltage ripple values.

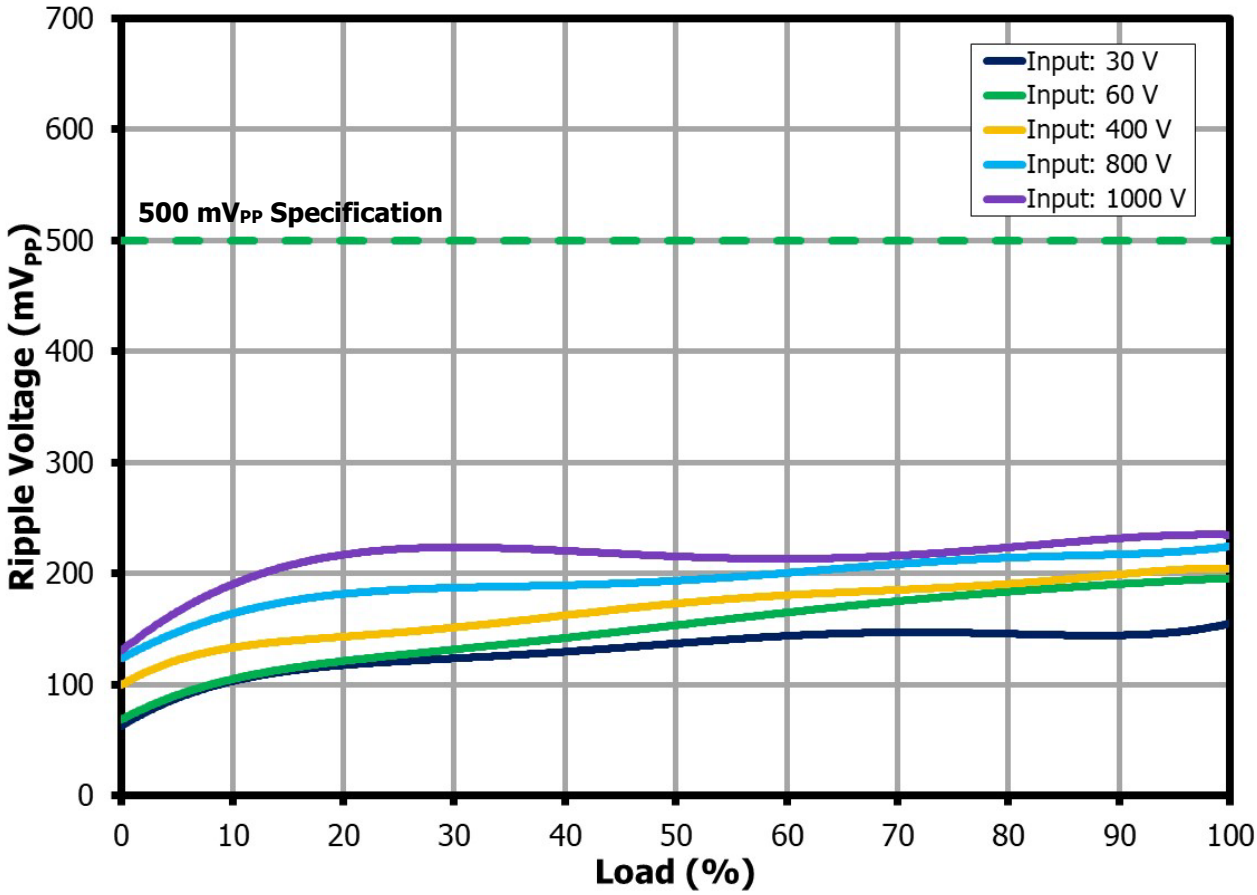


Figure 85 – Output Ripple Voltage (-40 °C Ambient).

[22] 74.66 mV_{PP} is the average value of the difference between the output voltage ripple measurements obtained while using a short and extended probe at 25 °C ambient temperature.

12 Diagnostic Circuit

The diagnostic circuit was tested by applying the following signals and settings:

PSU_CHECK: 3.3 V and 5 V
PGOOD_DETECT: 5 V with 500 Ω pull up resistor (10 mA)
7.5 V Output: No-load and full load (10 W)

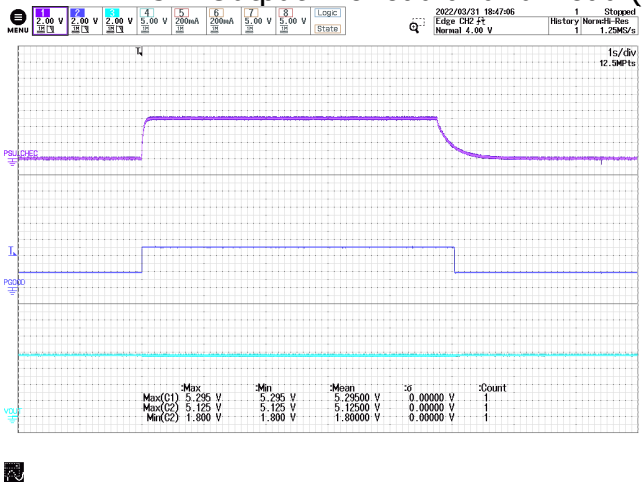


Figure 86 – Diagnostic Circuit.
PSU_CHECK = 5 V, PGOOD_DETECT = 5 V, No-Load.
CH1: V_{PSU_CHECK}, 2 V / div.
CH2: V_{PGOOD_DETECT}, 2 V / div.
CH3: V_{OUT}, 2 V / div.

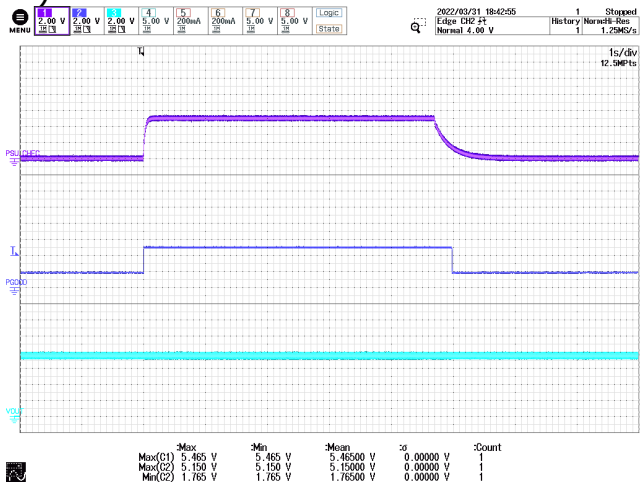


Figure 87 – Diagnostic Circuit.
PSU_CHECK = 5 V, PGOOD_DETECT = 5 V, Full Load.
CH1: V_{PSU_CHECK}, 2 V / div.
CH2: V_{PGOOD_DETECT}, 2 V / div.
CH3: V_{OUT}, 2 V / div.

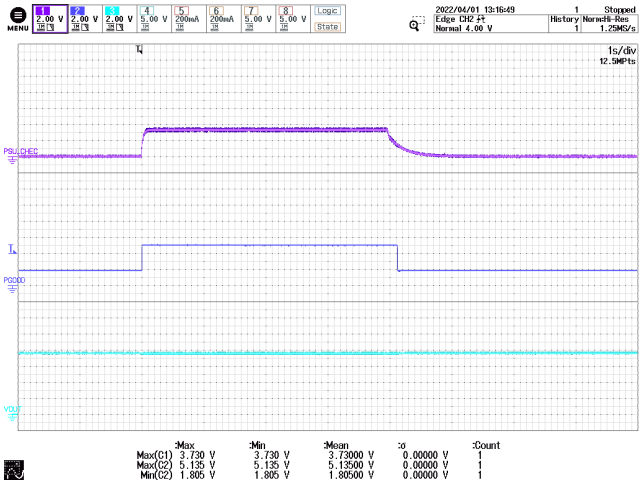


Figure 88 – Diagnostic Circuit.
PSU_CHECK = 3.3 V, PGOOD_DETECT = 5 V, No-Load.
CH1: V_{PSU_CHECK}, 2 V / div.
CH2: V_{PGOOD_DETECT}, 2 V / div.
CH3: V_{OUT}, 2 V / div.

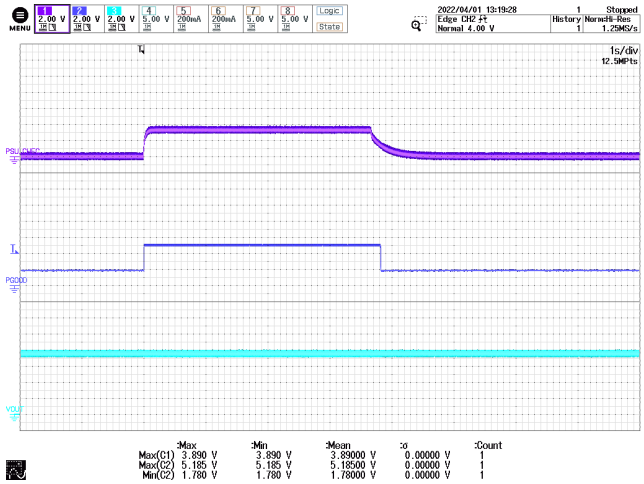


Figure 89 – Diagnostic Circuit.
PSU_CHECK = 3.3 V, PGOOD_DETECT = 5 V, Full Load.
CH1: V_{PSU_CHECK}, 2 V / div.
CH2: V_{PGOOD_DETECT}, 2 V / div.
CH3: V_{OUT}, 2 V / div.

13 Revision History

Date	Author	Revision	Description & Changes	Reviewed
28-Apr-22	JB	1.0	Initial Release.	Apps & Mktg
22-Jul-22	JB	1.1	Updated Figure 5 and 19. Updated sections 2.2, 6, 7.5 and 9.1. Added Ambient Waveforms.	Apps & Mktg
31-Jul-23	JS	2.0	Updated and added sections and figures for the data at -40 °C ambient temperature test condition.	Apps & Mktg

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