

Energy-Efficient Peak-Current Controlled Power Conversion IC Family Delivers 3 to 28 Watts in Universal-Input Flyback Power Supplies

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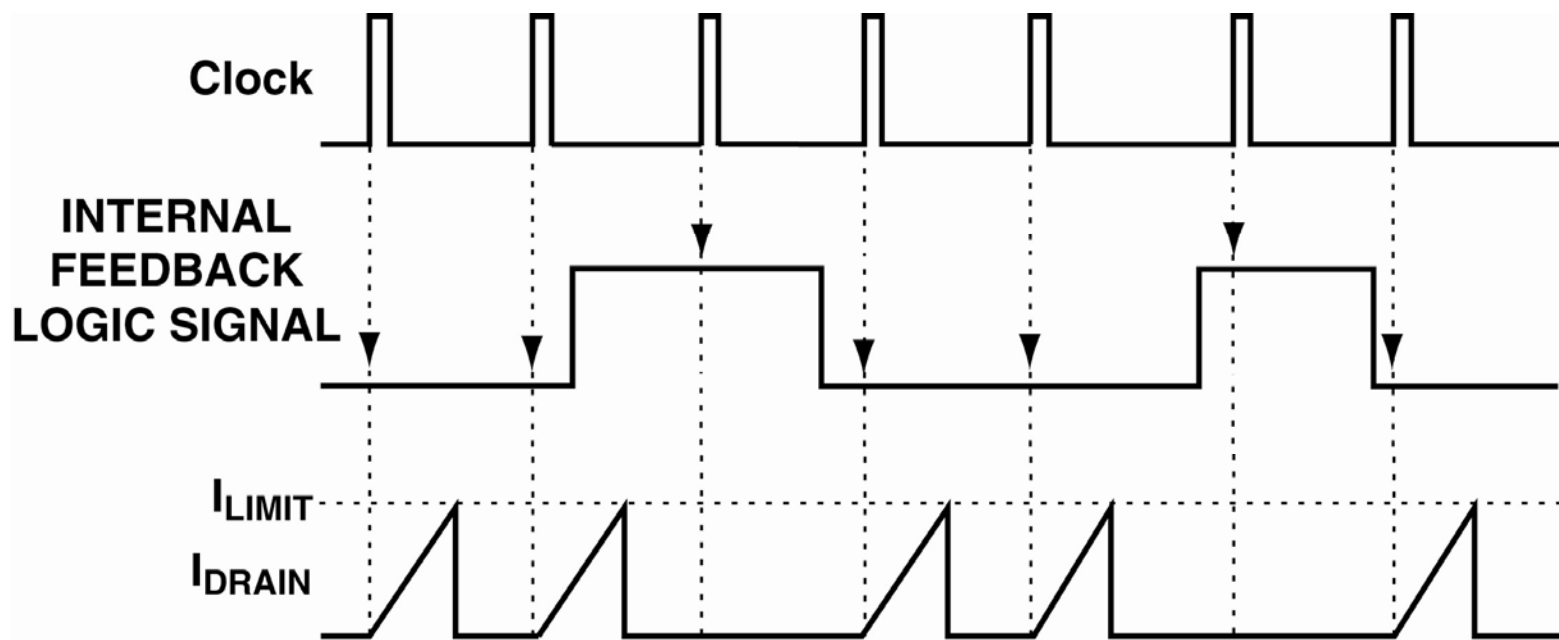


Scope of Paper and Presentation

- **Introduction of IC control scheme concept and its benefits**
- **IC operation and power supply interaction**
- **Defining the state machine state-change criteria and limits**
- **Descriptions of IC pin functionality & important internal functions**
- **Power supply performance results**
- **Conclusion**

Introduction: Basic IC Functionality

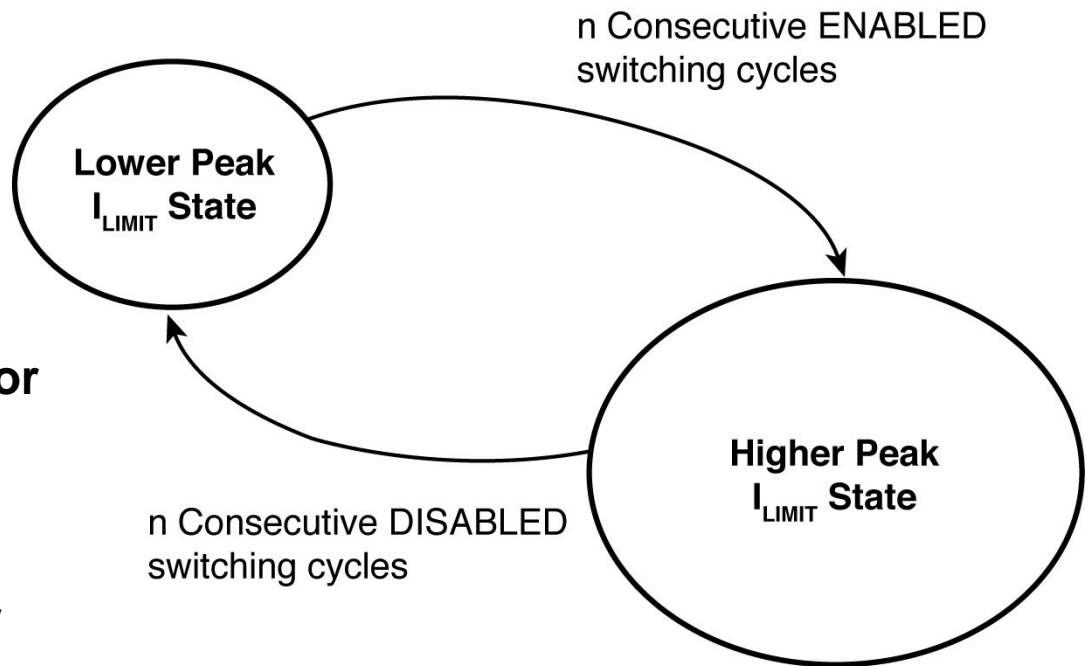
- ON/OFF control enables/disables MOSFET switching cycles
- Since MOSFET & controller are integrated, I_{DRAIN} is sensed directly
- Enabled cycle switch on-time ends when I_{DRAIN} reaches I_{LIMIT}



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Basic Functionality Continued: State Machine Operation and Supply Stability/Responsiveness

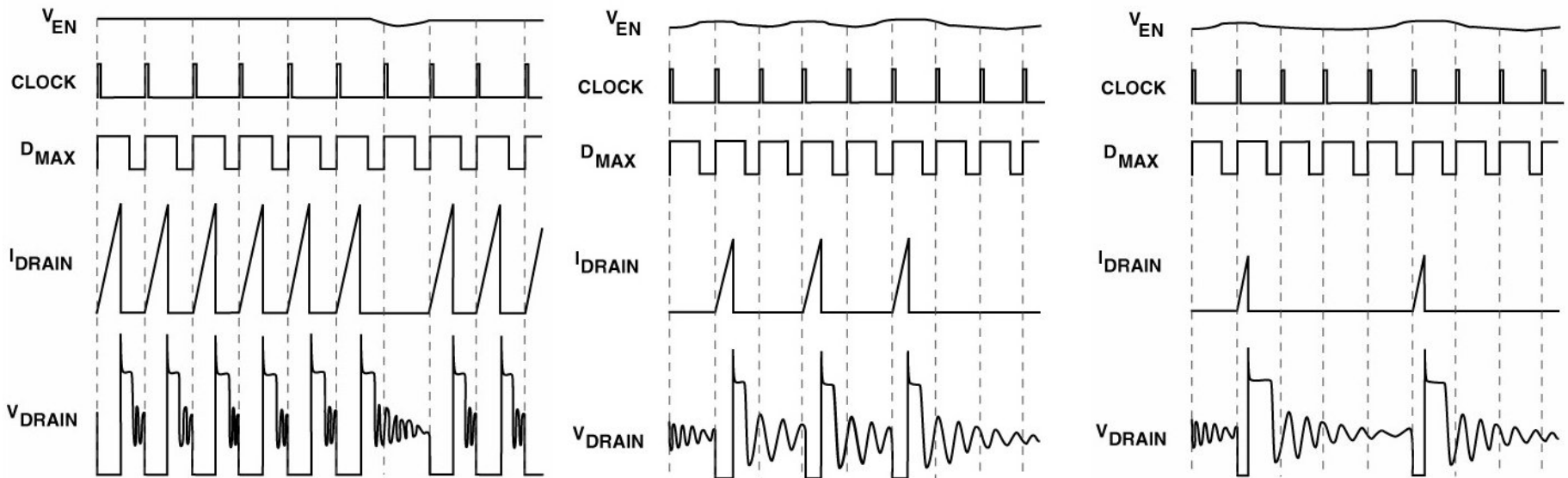
- State machine adjusts I_{LIMIT} based on number of consecutive enabled or disabled cycles
- Pole-zero placement, slope compensation and gain/phase bode plotting are eliminated
- Transient load responsiveness is fast yet stable, and equal to or better than that of a well compensated PWM controlled power supply



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State Machine Operational Overview & Benefits

- Since cycles are skipped while $V_{OUT} >$ the reference set point, ON/OFF control realizes very low no-load power consumption
- The state machine automatically adjusts the MOSFET I_{LIMIT} according to the load
 - (I_{LIMIT} is raised as the load increases and lowered as the load decreases)



Defining State-Machine State-Change Limits

- **Frequency boundary between CCM and DCM operation**

- The boundary frequency between CCM and DCM operation of a peak current limited, ON/OFF controlled, flyback converter is determined by the steady-state minimum inductor current (I_{MIN}) as a function of I_{LIMIT}

$$(1) \quad I_{\text{min}} = I_{\text{LIMIT}} - \frac{(1-D)T_s V_o}{n_L L} = I_{\text{LIMIT}} - \frac{(V_{\text{in}} T_s - L(I_{\text{LIMIT}} - I_{\text{min}}))V_o T_s}{n_L V_{\text{in}} T_s L} = I_{\text{LIMIT}} - \frac{T_s}{L} \left(\frac{V_o}{n_L} \parallel V_{\text{IN}} \right)$$

- where $1:n_L$ is the transformer primary to secondary turns ratio, T_s is the switching period (1/frequency), L is the primary winding inductance value, V_{IN} and V_o are the input and output voltages and D is the duty cycle.

Solving for the inductance at which $I_{\text{MIN}} = 0$ gives the CCM/ DCM boundary, and yields the critical switching frequency value of

$$(2) \quad f_{\text{crit}} = \frac{1}{I_{\text{LIMIT}} L} \left(\frac{V_o}{n_L} \parallel V_{\text{IN}} \right)$$

State-Machine State-Change Limits, continued

- **Power Delivery in DCM versus CCM**

- Power delivery in DCM is simply

$$(3) \quad P_{O,DCM} = \frac{1}{2} L I_{LIMIT}^2 f_s$$

- When operating in CCM, power delivery is a little more complex

$$(4) \quad P_{O,CCM} = V_o I_o = V_o \frac{(1-D)}{n_L} \left(\frac{I_{LIMIT} + I_{min}}{2} \right) = V_o \left(\frac{V_{IN}}{n_L V_{IN} + V_o} \right) \left(\frac{I_{LIMIT} + I_{min}}{2} \right) = \left(\frac{V_o}{n_L} \parallel V_{IN} \right) \left[I_{LIMIT} - \left(\frac{V_o}{n_L} \parallel V_{IN} \right) \left(\frac{1}{2L f_s} \right) \right]$$

- When a switching cycle is skipped in CCM and steady state operation ceases, the inductor current perturbation, $i_L^{\wedge}(0)$, must be taken into account. Thus, the inductor current, $I_{min-p}(i)$, at the end of the cycle following the skipped cycle is

$$(5) \quad I_{min-p}(i) = I_{min} + i_L^{\wedge}(0) \left(-\frac{V_o}{n_L V_{in}} \right)^i = I_{LIMIT} - \frac{T_s}{L} \left(\frac{V_o}{n_L} \parallel V_{IN} \right) + i_L^{\wedge}(0) \left(-\frac{V_o}{n_L V_{in}} \right)^i$$

and the power delivered in a train of m CCM switching cycles in time $(m+1)T_s$ following a perturbation, $i_L^{\wedge}(0)$, would thus be

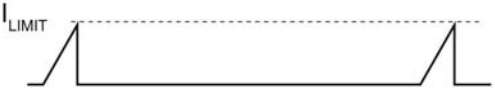



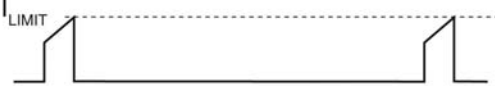

$$(6) \quad P_{O,CCM} = \frac{L}{2(m+1)T_s} \sum_{i=1}^m (I_{LIMIT}^2 - I_{min-p}^2(i)) = \frac{L}{2(m+1)T_s} \left[m I_{LIMIT}^2 - \sum_{i=1}^m \left(I_{LIMIT} - \frac{T_s}{L} \left(\frac{V_o}{n_L} \parallel V_{IN} \right) + i_L^{\wedge}(0) \left(-\frac{V_o}{n_L V_{IN}} \right)^i \right)^2 \right]$$

Defining State Machine State-Change Criteria

| Case | Power & f_s are minimum. Pertinent to the intermediate and the full I_{LIMIT} states | Power delivery and f_s are at a maximum. Pertinent to the intermediate I_{LIMIT} states and the lowest I_{LIMIT} state |
|--|---|---|
| DCM only | <p>One switching cycle followed by $(n-1)$ skipped cycles, $f_s = (\frac{1}{n})f_{clk}$, uses Equation 3:</p> $P_{min} = (\frac{1}{n})\frac{1}{2}LI_{LIM-state}^2 f_{clk}$ | <p>$(n-1)$ switching cycles followed by one skipped cycle, $f_s = (\frac{n-1}{n})f_{clk}$, uses Equation 3:</p> $P_{max} = (\frac{n-1}{n})\frac{1}{2}LI_{LIM-state}^2 f_{clk}$ |
| DCM @ min f_s CCM @ max f_s | <p>One switching cycle followed by $(n-1)$ skipped cycles, $f_s = (\frac{1}{n})f_{clk}$, uses Equation 3:</p> $P_{min} = (\frac{1}{n})\frac{1}{2}LI_{LIM-state}^2 f_{clk}$ | <p>$(n-1)$ switching cycles followed by one skipped cycle, in CCM (involves accounting for the perturbation as a result of the skipped cycle), uses Equation 6:</p> $P_{max} = \frac{L}{2(n)T_{clk}}[(n-1)I_{LIM}^2 - \sum_{i=1}^{n-1}(I_{LIM} - \frac{T_s}{L}(\frac{V_0}{n_L} \ V_{IN}) + i_L \hat{(0)}(-\frac{V_0}{n_L V_{IN}})^i)^2]$ |
| CCM only | <p>One switching cycle followed by $(n-1)$ skipped cycles, but $I_L \neq$ zero, even during $(n-1)$ skipped cycles. \therefore converter is always in CCM, $f_s = (\frac{1}{n})f_{clk}$, uses Equation 4:</p> $P_{min} = (\frac{V_o}{n_L} \ V_{IN})[I_{LIM-state} - (\frac{V_o}{n_L} \ V_{IN})(\frac{n}{2Lf_{clk}})]$ | <p>$(n-1)$ switching cycles followed by one skipped cycle, in CCM (involves accounting for the perturbation as a result of the skipped cycle), uses Equation 6:</p> $P_{max} = \frac{L}{2(n)T_{clk}}[(n-1)I_{LIM}^2 - \sum_{i=1}^{n-1}(I_{LIM} - \frac{T_s}{L}(\frac{V_0}{n_L} \ V_{IN}) + i_L \hat{(0)}(-\frac{V_0}{n_L V_{IN}})^i)^2]$ |

f_{clk} is the internal IC oscillator (clocking) frequency

State Machine State-Change Criteria Depicted

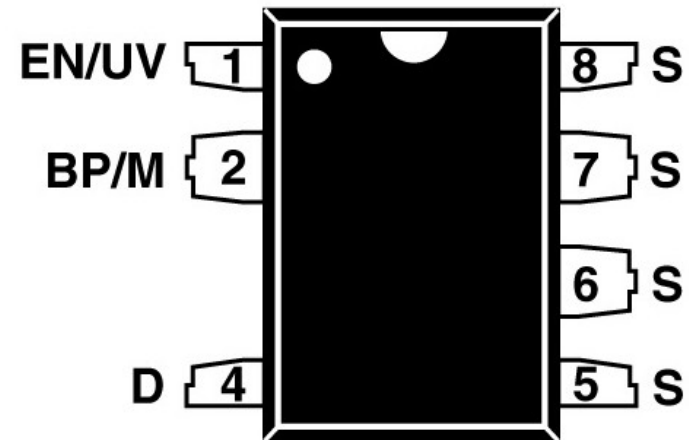
| CASE | Power delivery and f_s are minimum. Pertinent to the intermediate and the highest I_{LIMIT} state. | Power delivery and f_s are maximum. Pertinent to the intermediate and the lowest I_{LIMIT} state. |
|------------------------------------|---|--|
| DCM Only | <p style="text-align: center;">EQUATION 3</p>  <p style="text-align: center;">1 ENABLED, n DISABLED</p> | <p style="text-align: center;">EQUATION 3</p>  <p style="text-align: center;">n ENABLED, 1 DISABLED</p> |
| DCM @ min f_s CCM @ max f_s | <p style="text-align: center;">EQUATION 3</p>  <p style="text-align: center;">1 ENABLED, n DISABLED</p> | <p style="text-align: center;">EQUATION 6</p>  <p style="text-align: center;">n ENABLED, 1 DISABLED</p> |
| CCM Only | <p style="text-align: center;">EQUATION 4</p>  <p style="text-align: center;">1 ENABLED, n DISABLED</p> | <p style="text-align: center;">EQUATION 6</p>  <p style="text-align: center;">n ENABLED, 1 DISABLED</p> |

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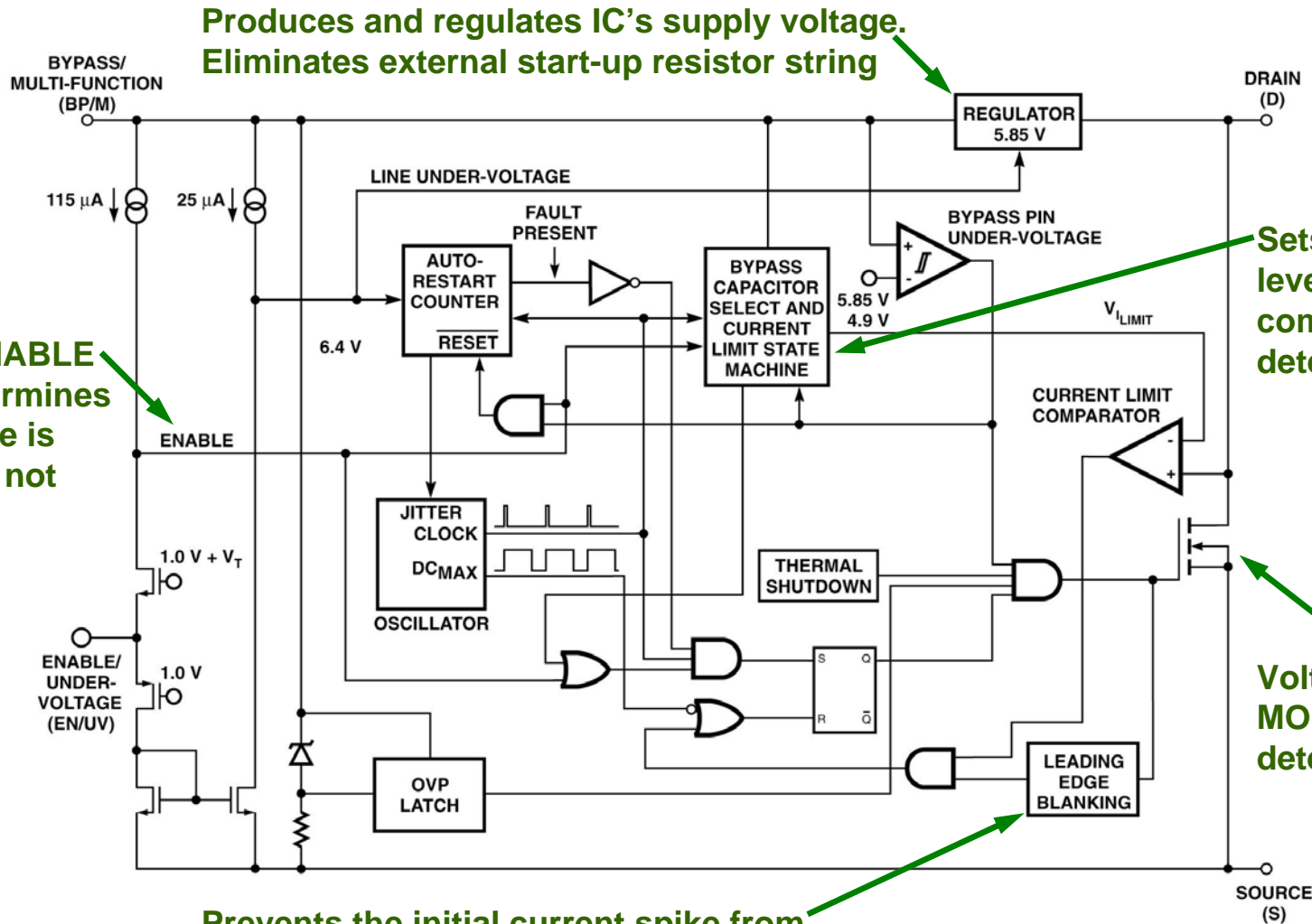
IC Pin Function Descriptions

- **DRAIN (D) Pin:**
 - Power MOSFET drain and high-voltage current source (start up circuit) connections
- **BYPASS / MULTI-FUNCTION (BP/M) Pin:**
 - Bias supply bypass capacitor connection point
 - Internal I_{LIMIT} level selection function
 - Input for latching shutdown function
- **ENABLE / UNDER-VOLTAGE (EN/UV) Pin:**
 - Feedback input to switching controller
 - Input for under-voltage lockout function
- **SOURCE (S) Pin:**
 - Power MOSFET source connections and controller ground reference point

P Package (DIP-8C)
G Package (SMD-8C)



Internal IC Circuitry and Functionality



Produces and regulates IC's supply voltage.
Eliminates external start-up resistor string

Internal ENABLE signal determines if next cycle is skipped or not

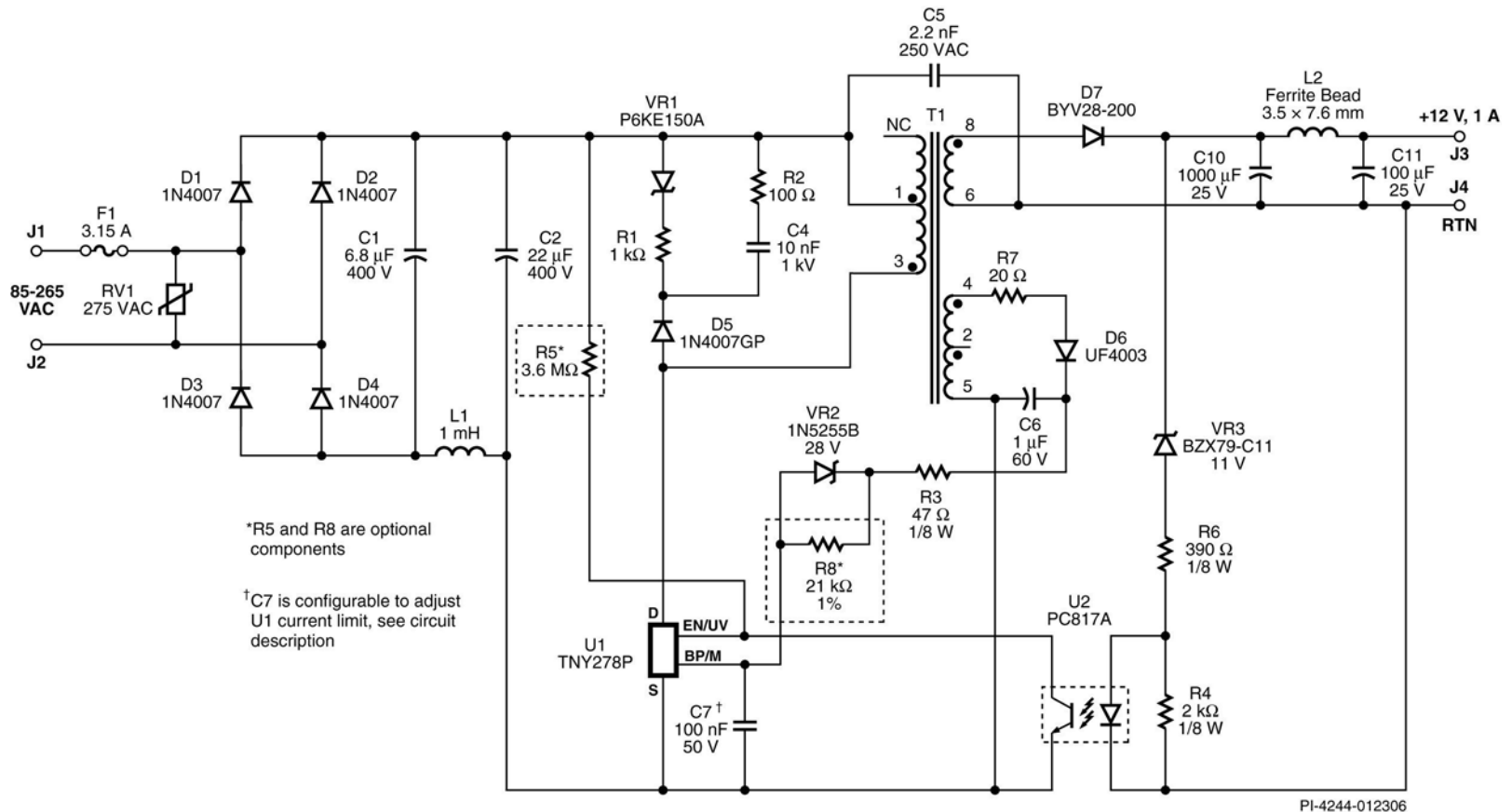
Sets voltage level used by comparator to detect I_{LIMIT}

Voltage across MOSFET D-S detects I_{LIMIT}

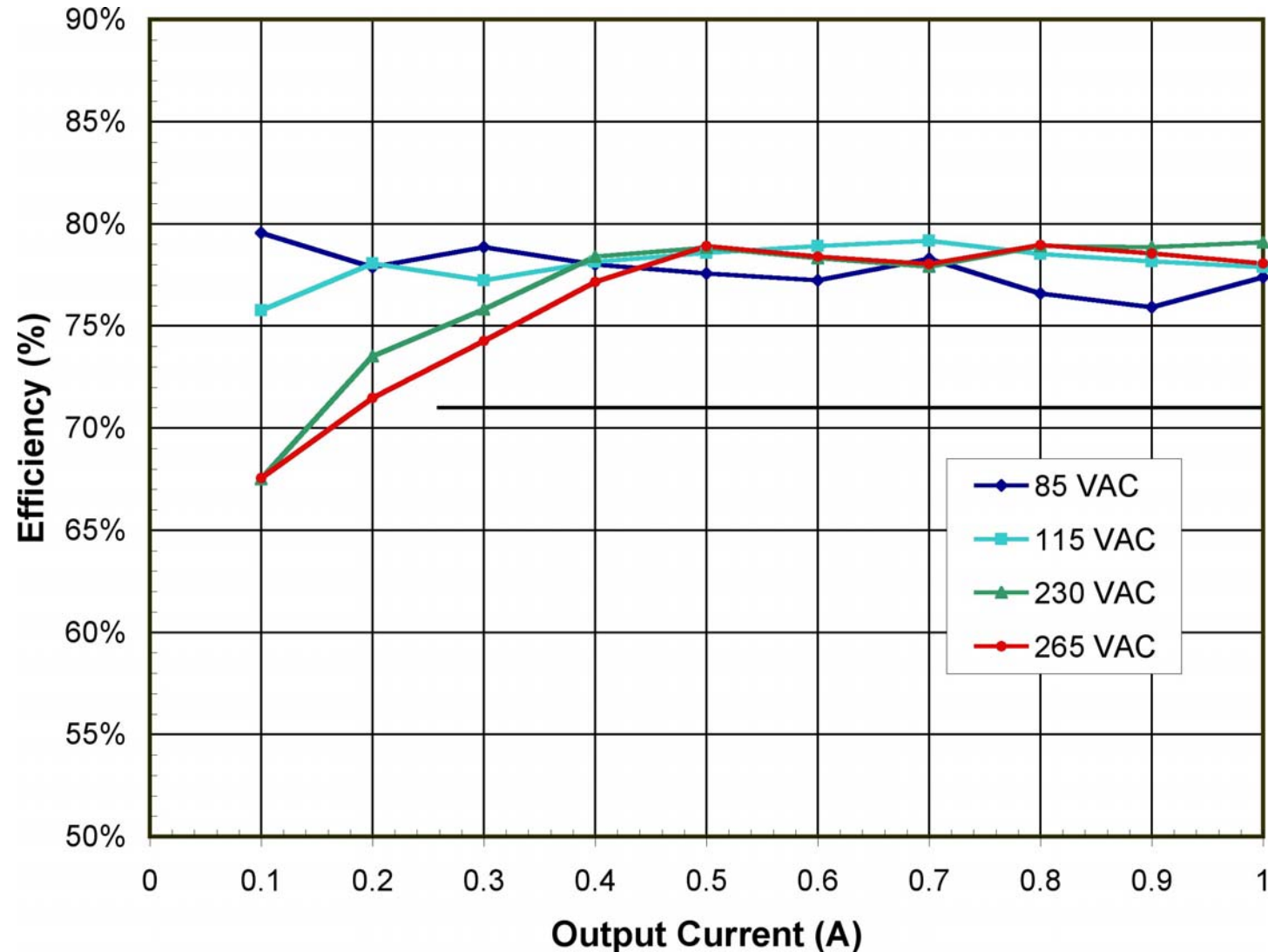
Prevents the initial current spike from falsely triggering the I_{LIMIT} comparator

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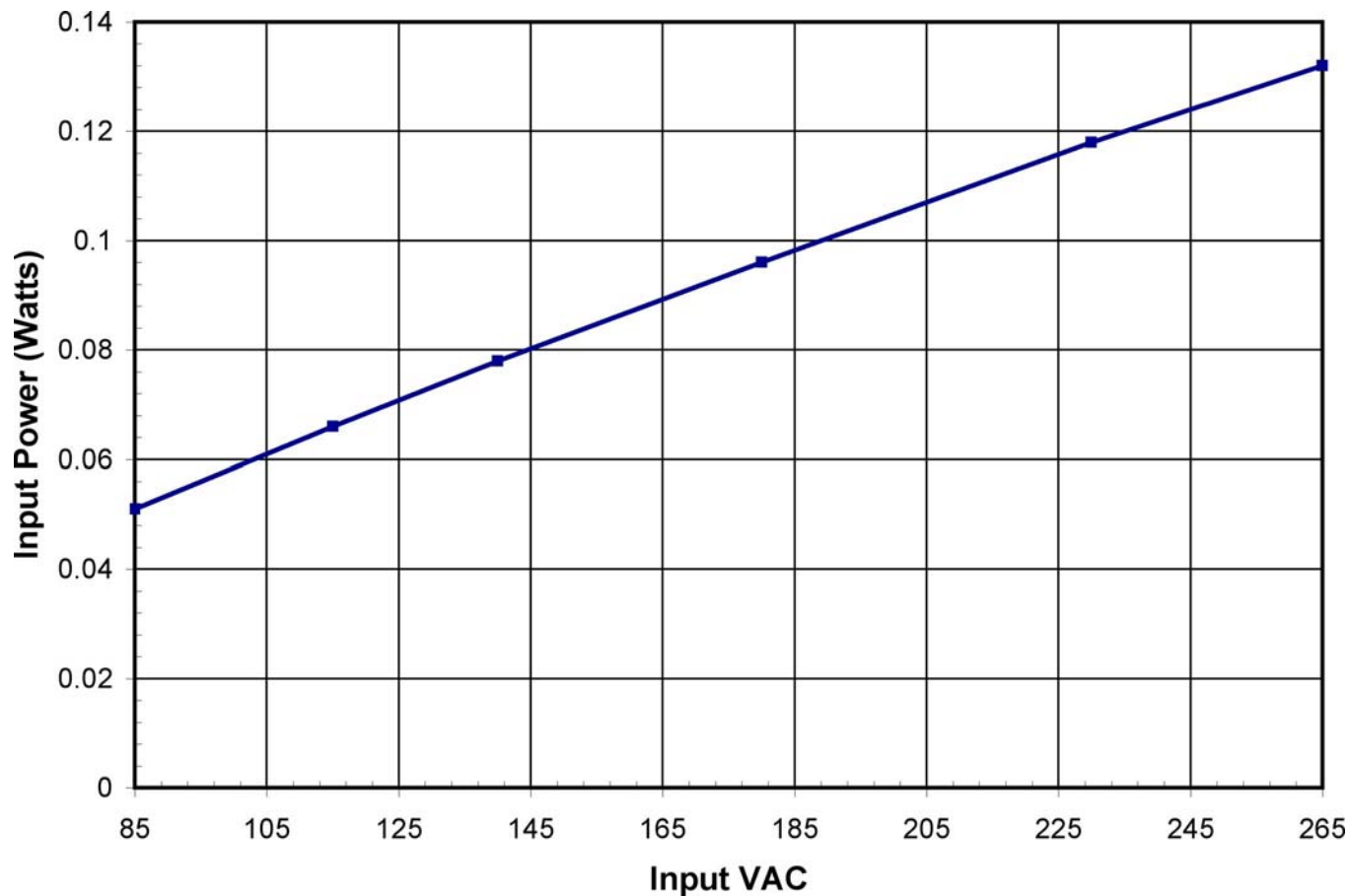
Flyback Converter Designed Around the IC



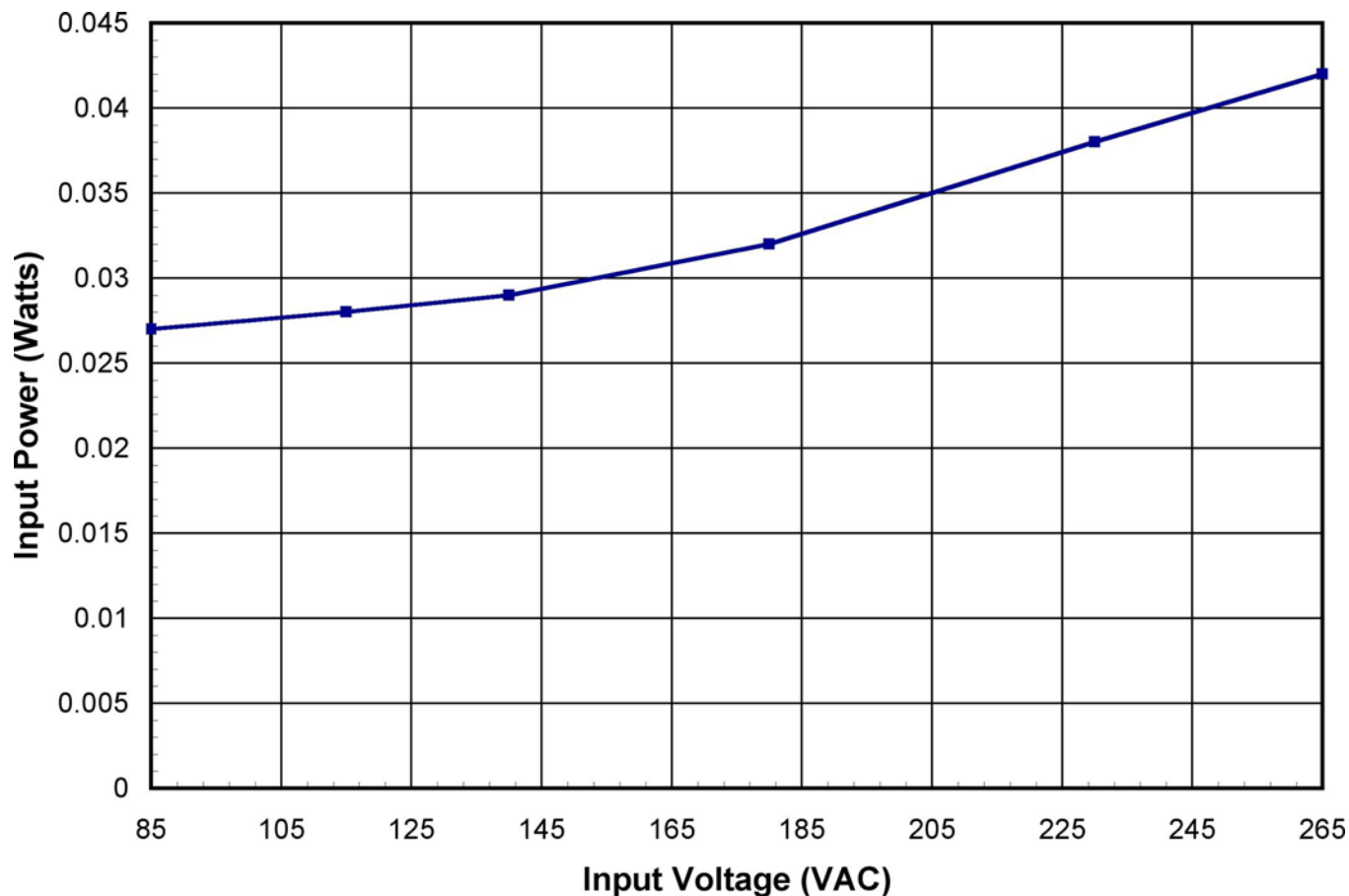
Power Supply Performance Results: Efficiency



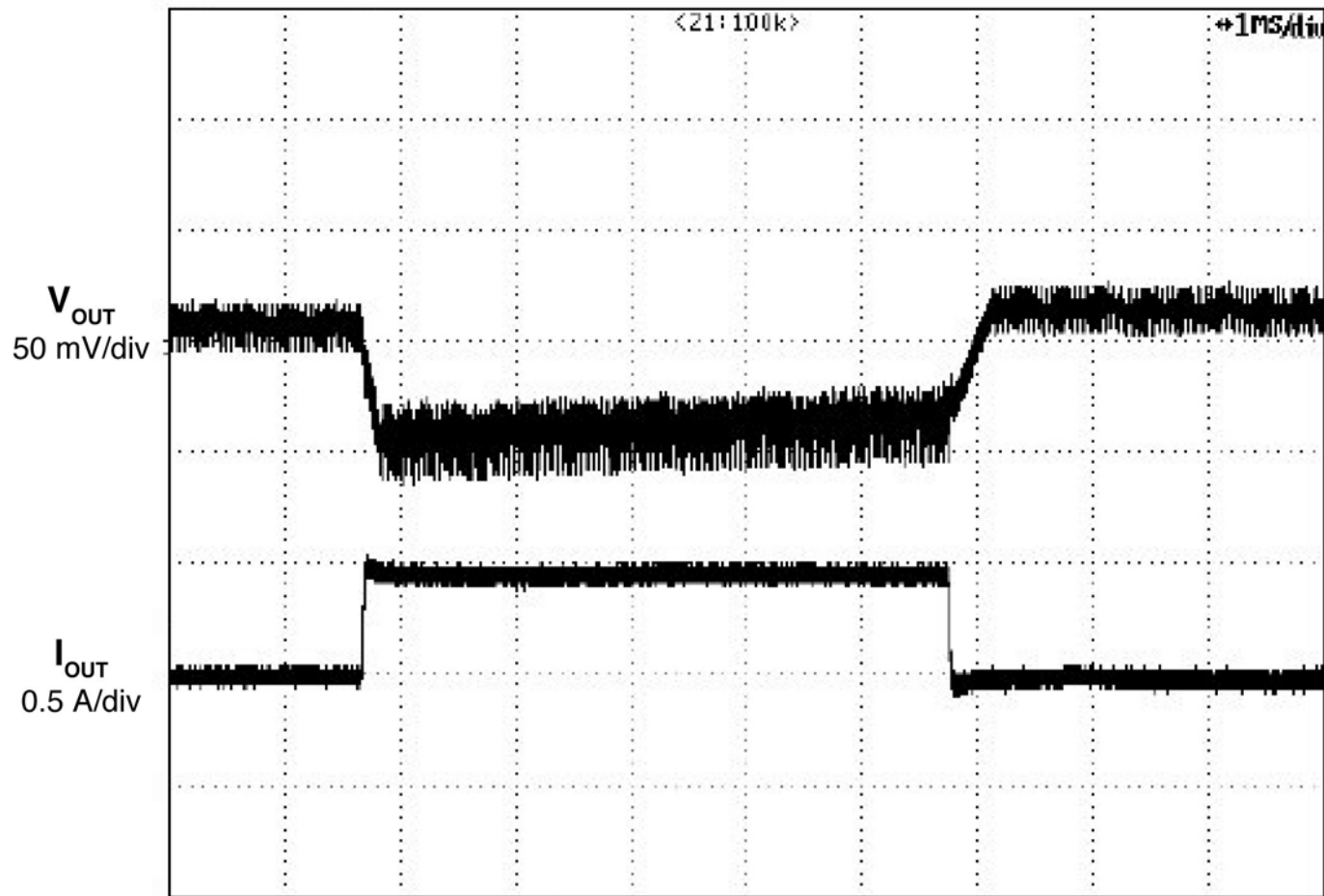
Power Supply Performance Results: No-load Power Consumption without a Bias Winding



Power Supply Performance Results: No-load Power Consumption with a Bias Winding

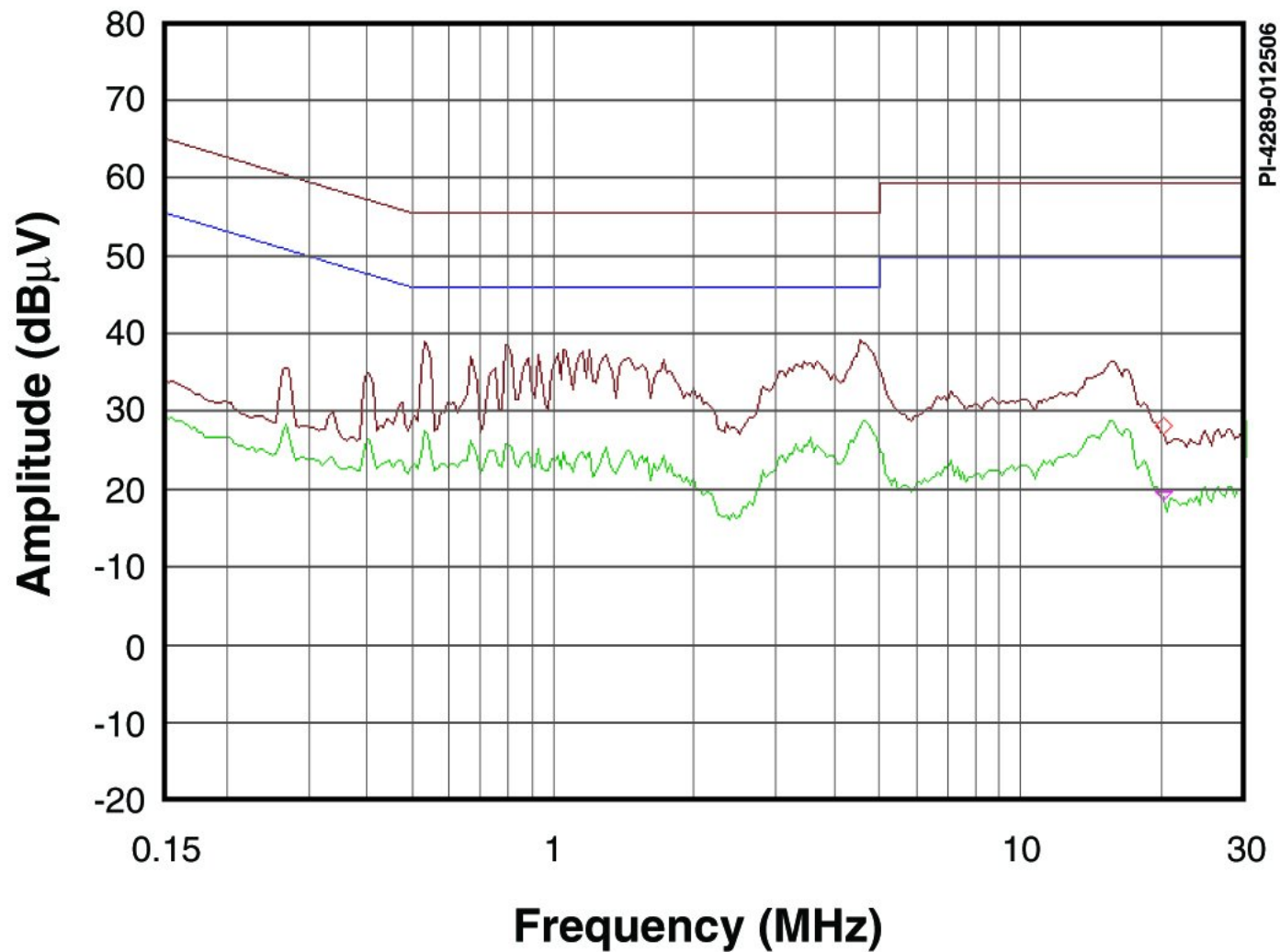


Power Supply Performance Results: Transient Load Response



10 ms at 1 ms/div

Power Supply Performance Results: Conducted EMI



Conclusion

- **Integrating a high-voltage MOSFET with a simple controller:**
 - Shortens the duration and the cost of the design process
 - Enables the integration of functionality that is otherwise impossible
- **ON/OFF control and the state machine give the following benefits:**
 - Consistently high active-mode efficiency over the entire load range
 - Very low light load and no-load power consumption
 - Delivers optimized responsiveness without the loop compensation exercise
 - Eliminates audible sound production at no-load and light loading
- **Careful Modeling of state machine state-change criteria and limits:**
 - Minimized the number of I_{LIMIT} levels required & kept change criteria simple
 - Enabled excellent transient load response without unnecessary state changes
- **Power supply performance results show that the concept is sound**
 - Low cost, good performing power supplies can be quickly designed