

DI-40 Design Idea

DPA-Switch®

2.5 V, 20 W DC-DC Converter with Synchronous Rectification

Application	Device	Power Output	Input Voltage	Output Voltage	Topology
DC-DC Converter	DPA424R	20 W	36 – 75 VAC	2.5 V	Forward

Design Highlights

- Extremely low component count
- High efficiency – 86% using synchronous rectification
- No current sense resistor or current transformer required
- Output overload, open loop and thermal protection
- Accurate input under/overvoltage meets ETSI standards
- 300 kHz switching frequency – optimizes efficiency when simple self-driven synchronous rectification is used

Operation

DPA-Switch greatly simplifies the design compared to a discrete implementation. Resistor R1 programs the input UV/OV thresholds. The tight tolerance of the UV/OV thresholds limits the range of gate drive voltages applied to MOSFETs Q1 and Q2, eliminating the need for gate voltage clamp circuitry. The self-driven synchronous rectification configuration is therefore very simple, with R13

filtering voltage spikes at the gate of Q2, and D3 preventing the body diode of Q1 from conducting.

Capacitor C8 and the gate capacitance of Q1 reset T1 during DPA-Switch off-time. Zener VR1 provides a hard voltage clamp to limit DRAIN voltage under output transient and overload conditions.

Since the output voltage is low, the U2 LED is supplied with a higher voltage derived from a winding on output choke L2.

The DPA-Switch bias supply is derived from a forward winding on transformer T1. Flyback windings are not recommended for this purpose, since the bias capacitor C4 would create high capacitive loading during DPA-Switch off-time, preventing the transformer from efficiently resetting.

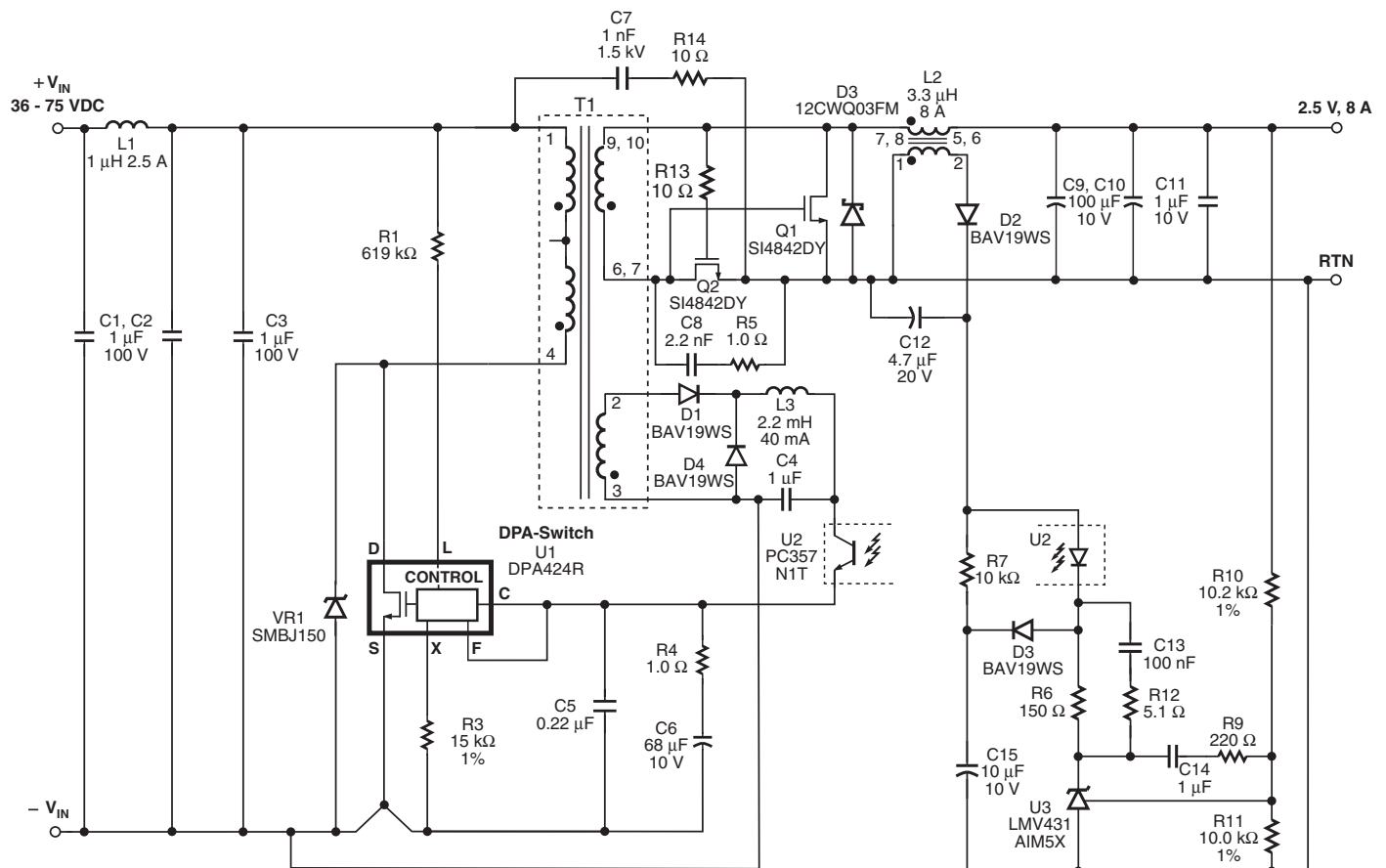


Figure 1. DPA-Switch 20 W DC-DC Converter.

PI-3264-051303

Key Design Points

- For nominal under-voltage set point V_{UV} :
 $R1 = (V_{UV} - 2.35 \text{ V}) / 50 \mu\text{A}$. $V_{OV} = (R1 \times 135 \mu\text{A}) + 2.5 \text{ V}$.
- Locate C5, C6, and R4 close to U1 CONTROL pin, with ground connected to SOURCE pin.
- Minimize primary and secondary layout loop area to reduce parasitic inductance.
- Optocoupler U2 should have controlled CTR of 100-200% for optimum loop stability.
- Size transformer reset components C8 and R5, and the Q1 gate capacitance to assure transformer reset at minimum operating voltage without exceeding 170 V drain voltage at high line.

- Set Zener VR1 clamp voltage to 150 V to guarantee both transformer reset and limit DRAIN voltage below BV_{DSS} .
- Scale primary side forward bias winding to provide 12 V to 15 V at minimum input voltage, nominal load.
- Secondary choke winding provides 5 V at nominal load.
- Main primary power return should be connected to the DPA-Switch tab, not to the SOURCE pin.
- Consult AN-31 for additional design tips.

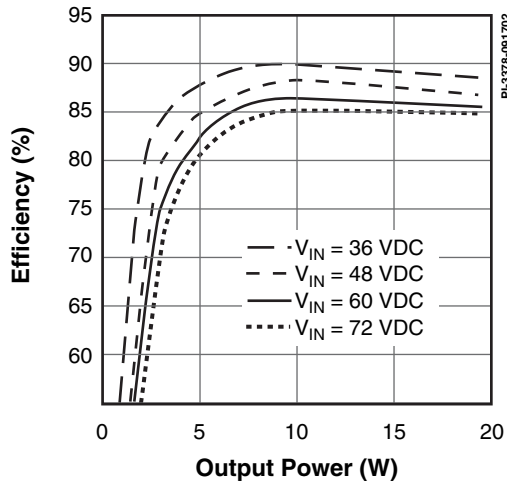


Figure 2. Efficiency vs. Output Power.

Transformer Parameters

Core Material	PR140 EPCOS N87 material ungapped
Bobbin	P1408 8 pin (B&B B-096 or equivalent)
Winding Details	Bias: 6T, 32 AWG Primary: 7T + 7T, 2 × 28 AWG Secondary: 2T, 4 × 26 AWG
Winding Order (pin numbers)	Bias: (3-2), tape Primary: (4-FL), tape Secondary: (6, 7-9, 10), tape Primary: (FL-10), tape
Primary Inductance	392 μH , $\pm 25\%$
Primary Resonant Frequency	3 MHz (minimum)
Leakage Inductance	1 μH (maximum)

Table 1. Transformer Parameters. (AWG = American Wire Gauge)

Output Inductor Parameters

Core Material	EPCOS N87 material, gap for AL of 206 nH/T ²
Bobbin	P1408 8 pin (B&B B-096 or equivalent)
Winding Details	Main: 4T, 4 × 26 AWG Bias: 10T, 32 AWG
Winding Order (pin numbers)	Main: (7, 8-5, 6), tape Bias: (1-2), tape
Inductance	Pin (5, 6-7, 8): 3.3 μH , $\pm 10\%$

Table 2. Output Inductor Design Parameters.

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