DI-187 Design Idea
TOPSwitch®-HX

35 W LCD Monitor

Application	Device	Power Output	Input Voltage	Output Voltage	Topology
LCD Monitor	TOP257EN	35 W	90 – 264 VAC	13 V	Flyback

Design Highlights

- Low component count, high efficiency
  - Delivers 35 W in 50 °C ambient temperature environments
- EcoSmart® multi-mode technology meets energy efficiency standards
  - 0.55 W output power for <1 W input
  - No-load power consumption: <200 mW at 230 VAC
  - >82% Full-load efficiency
- Uses new low profile eSIP-7C high-power package that reduces device height and PCB area
- 132 kHz switching frequency minimizes size and cost of power magnetics
- Integrated safety and reliability features
  - Accurate, auto-recovering hysteretic thermal shutdown maintains safe PCB temperatures in any condition
  - Auto-restart protects against output short circuits and open feedback loops
  - Output overvoltage protection (OVP), configurable for latching or self-recovery
  - Input undervoltage (UV) protection prevents power-up or power-down output glitches
  - Input overvoltage (OV) protection extends line surge limit
- Compliance to EN55022 and CISPR-22 Class B conducted EMI: >6 dB margin

Operation

The design schematic in Figure 1 shows an LCD monitor power supply utilizing the TOPSwitch-HX TOP257EN (U1) in a flyback configuration. This supply operates over a wide input range (90 to 264 VAC), delivering a 13 V, 35 W supply to the load.

Y-capacitors C1, C2, and C7 together with inductor L1 provide common mode filtering. Differential mode filtering is provided by X-capacitor C3 and by the bulk capacitor C4. The filtered AC goes to a bridge rectifier. Thermistor RT1 limits the inrush current when AC is applied.

IC U1 turns on when the current into the V pin exceeds 25 μA. Resistor R3 sets this input voltage threshold to 100 V DC.

IC U1 regulates the output by adjusting the duty cycle of the PWM controller which drives the integrated switching MOSFET. The controller within U1 uses a multi-mode control scheme which seemlessly transitions between different switching modes to maximize efficiency at any load.

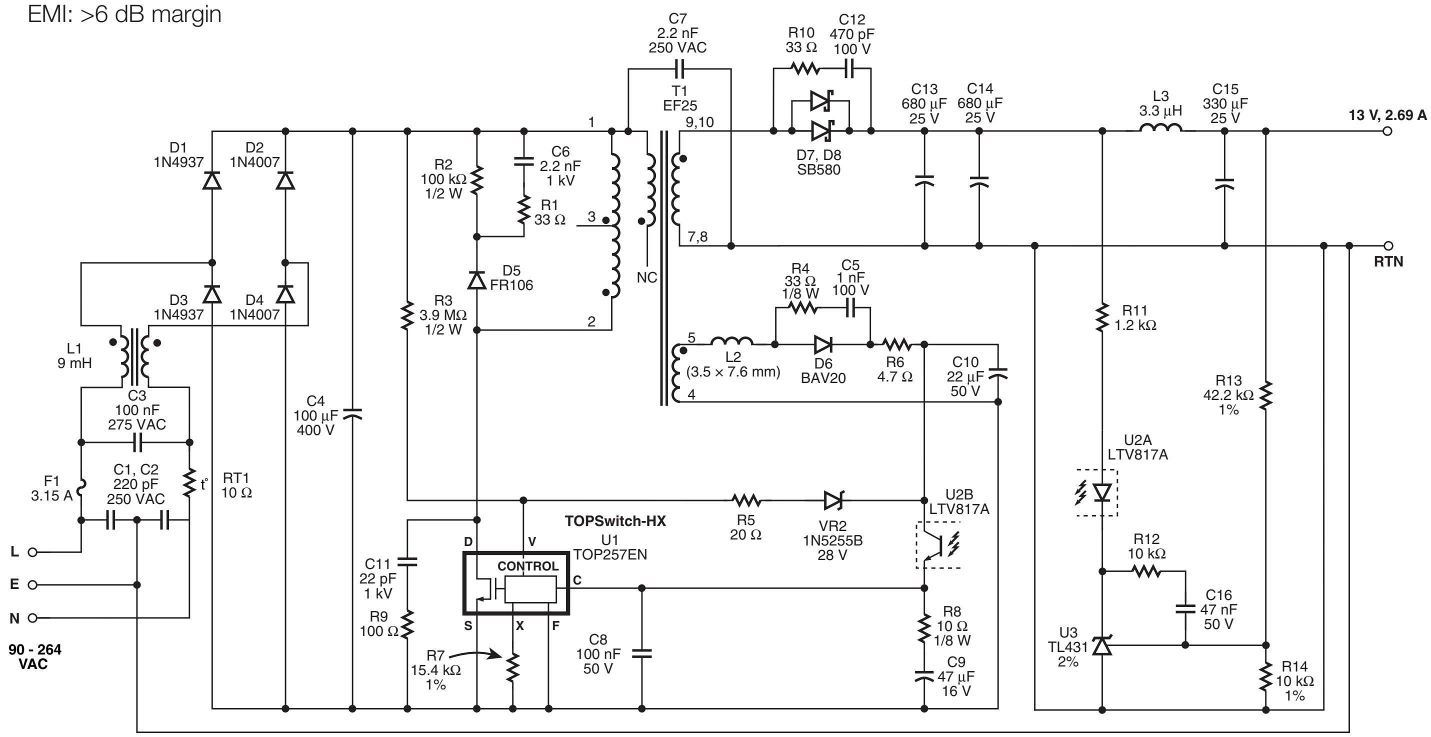

Figure 1. Schematic of a 35 W LCD Monitor Using TOP257EN.

A clamp network formed by D5, C6, R1, and R2 limits U1's drain voltage at turn-off. Fast-recovery diode D5 recovers some of the clamp energy; R1 limits reverse diode currents and dampens high-frequency ringing.

The output of the bias winding is rectified by D6 and filtered by C10. Zener diode VR2 and resistor R5 form a latching output overvoltage protection (OVP) circuit. Increased voltage at the output causes increased voltage across C10. In an overvoltage condition Zener VR2 breaks down and current flows into the V pin of IC U1, initiating a latching shutdown. The shutdown can be either latching or auto-recovering depending on the value of R5.

Diodes D7 and D8 rectify the secondary side output. Low-ESR capacitors (C13, C14) filter the output from D7 and D8. A second-order filter made up of L3 and C15 provides additional filtering on the output that switching noise across C13 and C14.

Resistors R13 and R14 act as a potential divider to sense the output voltage. U3 drives optocoupler U2 through resistor R11 to provide feedback information to U1's C pin.

Key Design Points

- Fast-recovery diodes D1 and D3 reduce radiated EMI (by eliminating voltage spikes inherent to regular diode high-frequency turn-off snap, and by not conducting AC line-induced noise). Their placement ensures one of the two conducts in each half cycle.
- Y-capacitor C7 placed across the transformer (T1) isolation barrier reduces conducted EMI. The switching frequency is modulated (jittered) to reduce EMI.

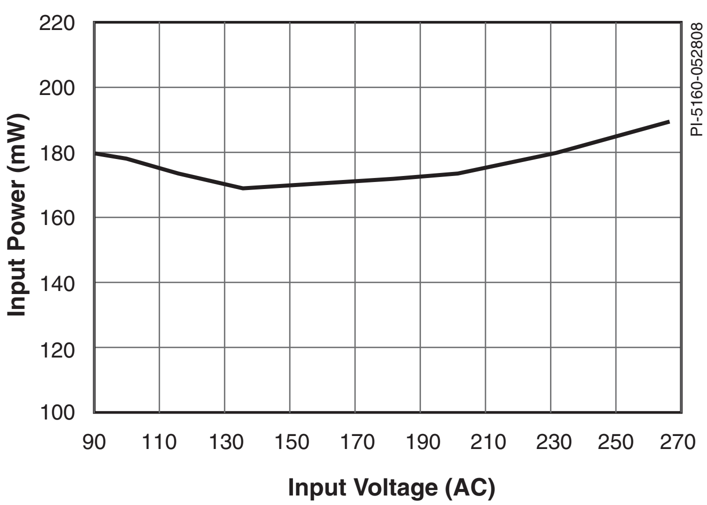

Figure 2. No-load Input Power vs Line Voltage.

- OVP may be configured for latching (as in this design) or for self recovery (non-latching). For non-latching recovery increase R5 to 5.1 kΩ.
- Resistor R4 and C5 form a snubber network across diode D6. With ferrite bead L2 they reduce high-frequency conducted and radiated EMI.

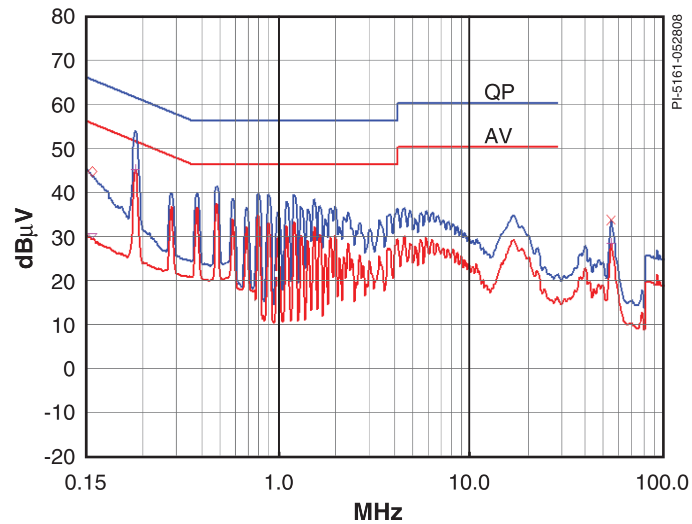

Figure 3. Conducted EMI with EN55022 B Limits. Input: 230 VAC, Maximum Steady-state Load.

Transformer Parameters

Core Material	EF25, gapped for ALG of 220 nH/t²
Bobbin	EF25 10 pins, Horizontal
Winding Details	First half primary: 29T, #26 AWG Bias/feedback: 8T × 4, #30 AWG Secondary: 7T × 2, #23, TIW Shield: 9T × 4, #39 AWG Second half primary: 27T, #26 AWG
Winding Order	First half primary (2–3), Bias/feedback (5–4), Secondary (9,10–7,8), Shield (NC–1), Second half primary (3–1)
Primary Inductance	690 μH, ±5%
Primary Resonant Frequency	1.8 MHz (minimum)
Leakage Inductance	13 μH (maximum)

Table 1. Transformer Parameters. (AWG = American Wire Gauge, TIW = Triple Insulated Wire, NC = No Connection)

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