

The voltage generated by the secondary of T1 is rectified by D1 and filtered by C3 to provide the 12 V output voltage. An LC post filter (C4, L1) is connected to this output in order to reduce switching frequency output ripple.

The output voltage is controlled using a TL431 voltage reference (U4). Resistor R4 provides the bias current for U4. Low frequency feedback to U4 is derived from a voltage divider network R5 and R8. The center point of this network is tied to the 2.5 V_{REF} pin of U4. Capacitor C8 and resistor R6 roll off the high frequency gain of U4. Resistor R9 sets the loop gain.

Key Design Points

- Design the RCD clamp (C2, R1 and D3) for normal operation, thereby maximizing efficiency at light load. Zener diode VR1 provides a defined maximum clamp voltage and typically only conducts during load transients or during an overload condition.
- A fast recovery diode such as a FR106, may be used in place of D3 to increase leakage inductance energy recovery and maximize efficiency.
- The power supply is designed to operate in continuous mode with a K_p of 0.5.
- The M pin is shorted to the SOURCE pin, programming the current limit to be equal to the internal device current limit.

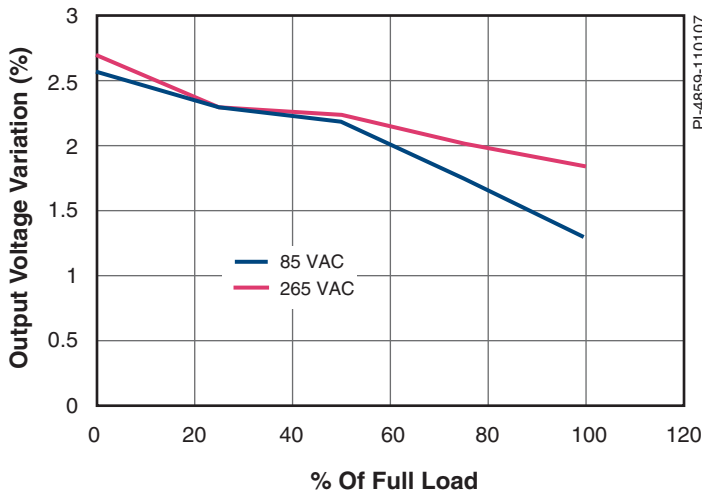


Figure 2. Worst Case Line and Load Regulation.

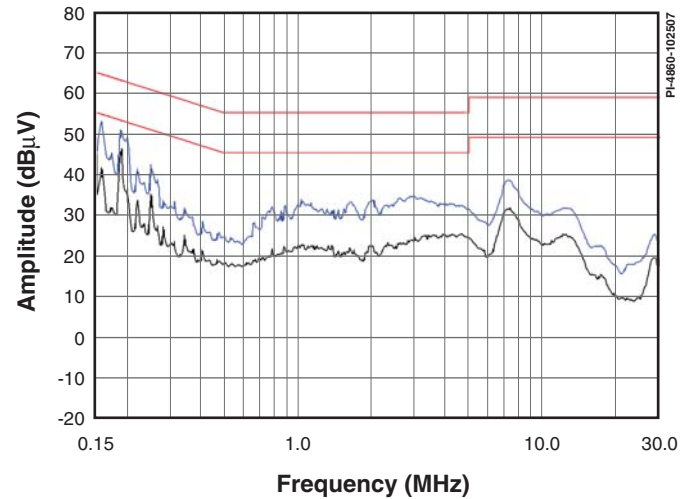


Figure 3. Worst Case Conducted EMI (230 VAC) Artificial Hand Connected to Output RTN.

Transformer Parameters

Core Material	EF25 NC-2H or equivalent, gapped for ALG of 141 nH/t ²
Bobbin	EF25, 10 pin, Horizontal
Winding Details	Primary: 41T × 1, 0.32 mm, tape Bias: 15T × 2, 0.32 mm, 3 layers, tape 12 V: 12T × 3, 0.40 mm (TIW), 3 layers tape Primary: 41T × 1, 0.32 mm, 2 layers tape
Winding Order	Primary-1 (3-2), Bias(5-4), 12 V (7-6), Primary-2 (2-1)
Primary Inductance	1030 µH, ±10%
Primary Resonant Frequency	700 kHz (minimum)
Leakage Inductance	30 µH (maximum)

Table 1. Transformer Parameters. (TIW = Triple Insulated Wire).

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